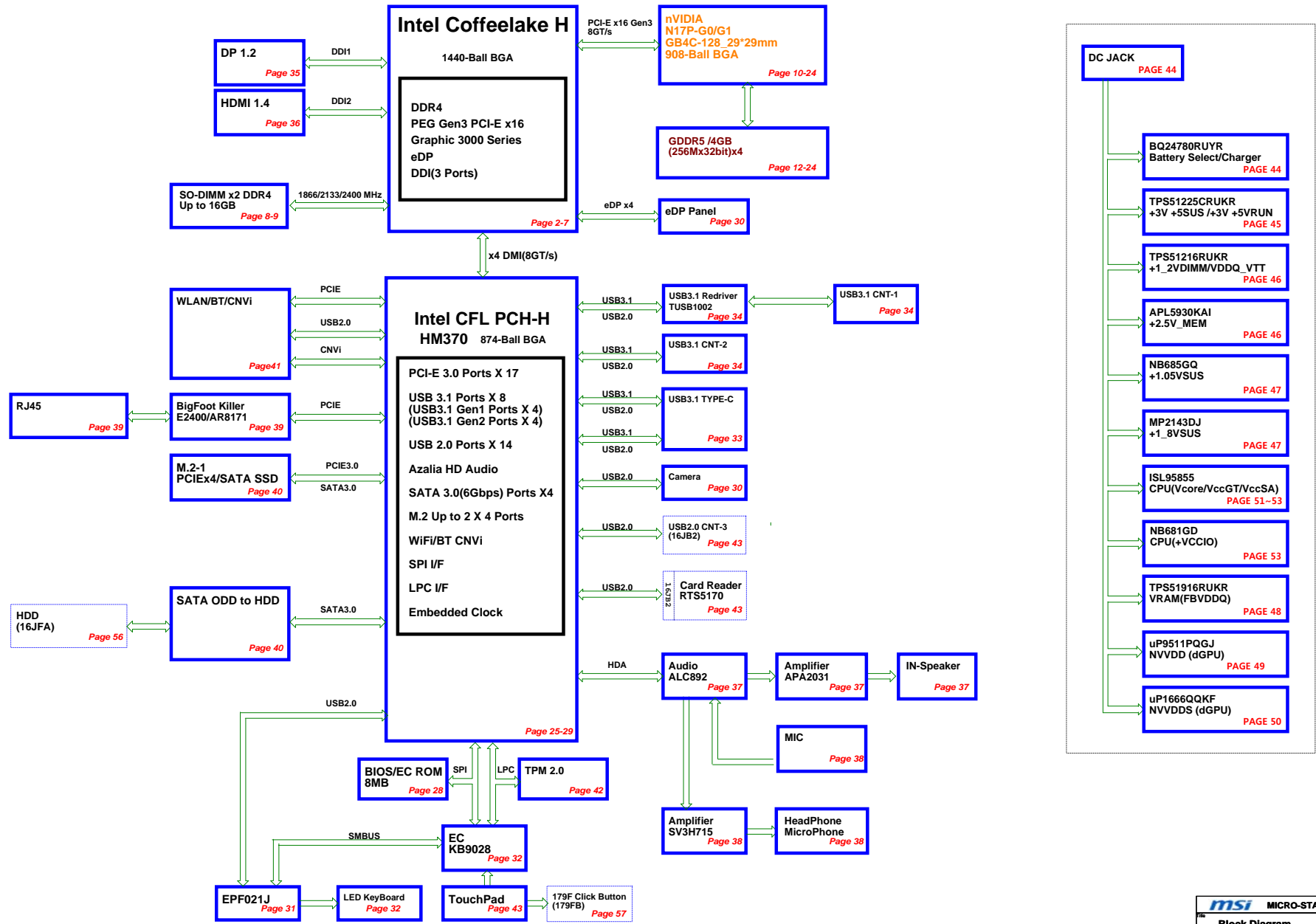


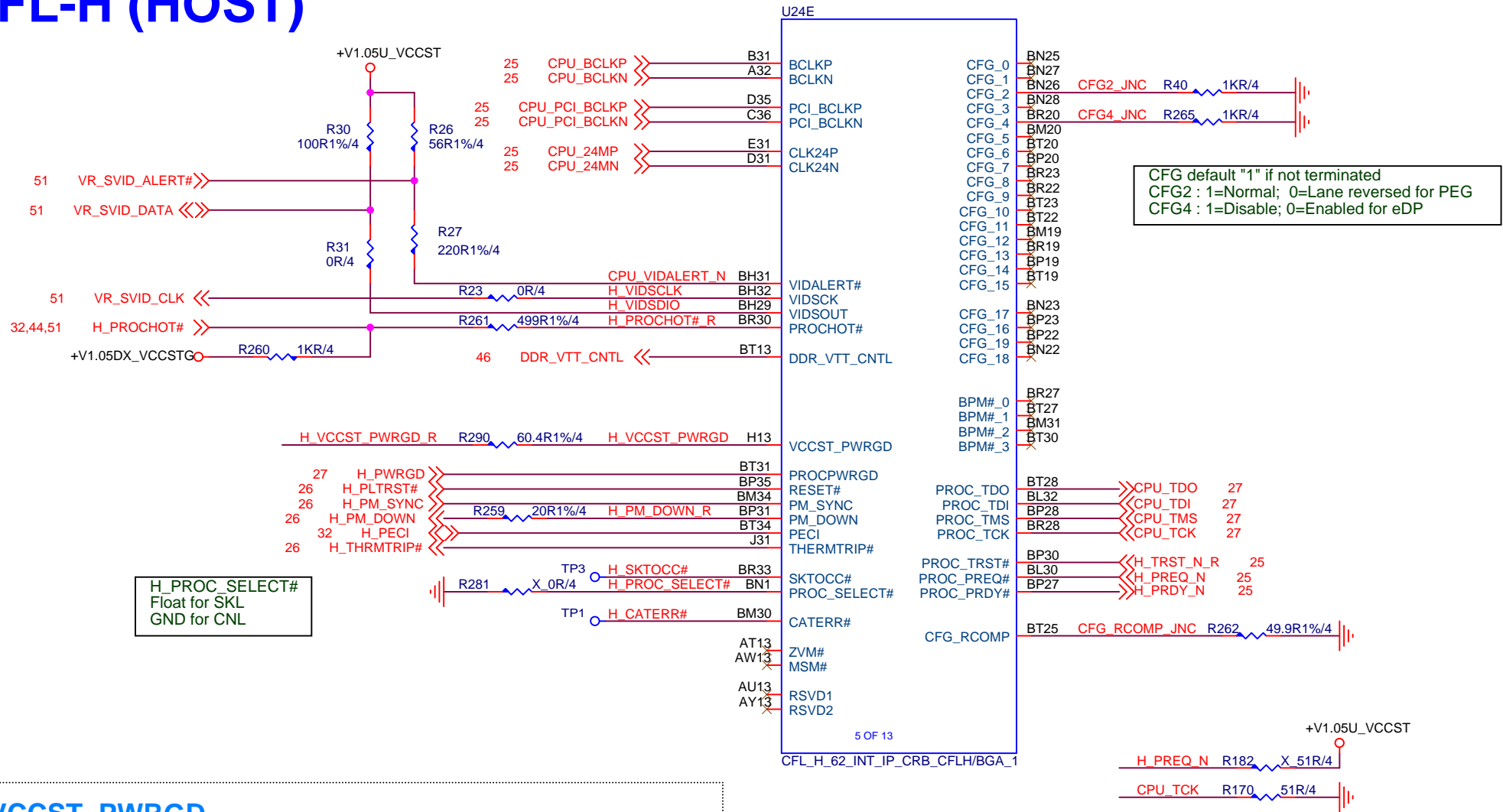
MS-16JF/MS-179F

Ver:0A

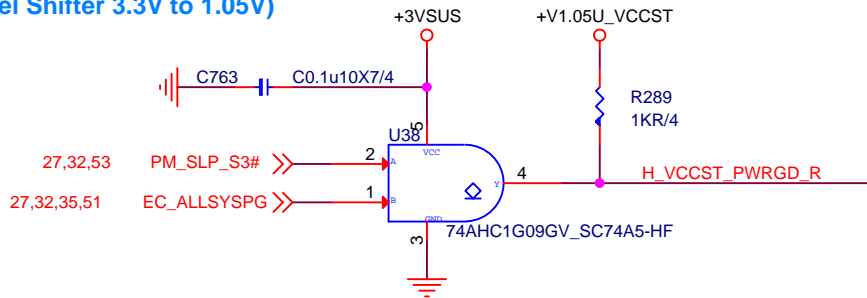
Intel CoffeeLake Mobile



CFL-H (HOST)

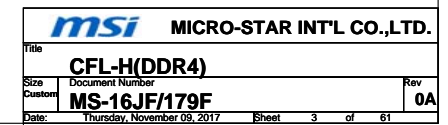


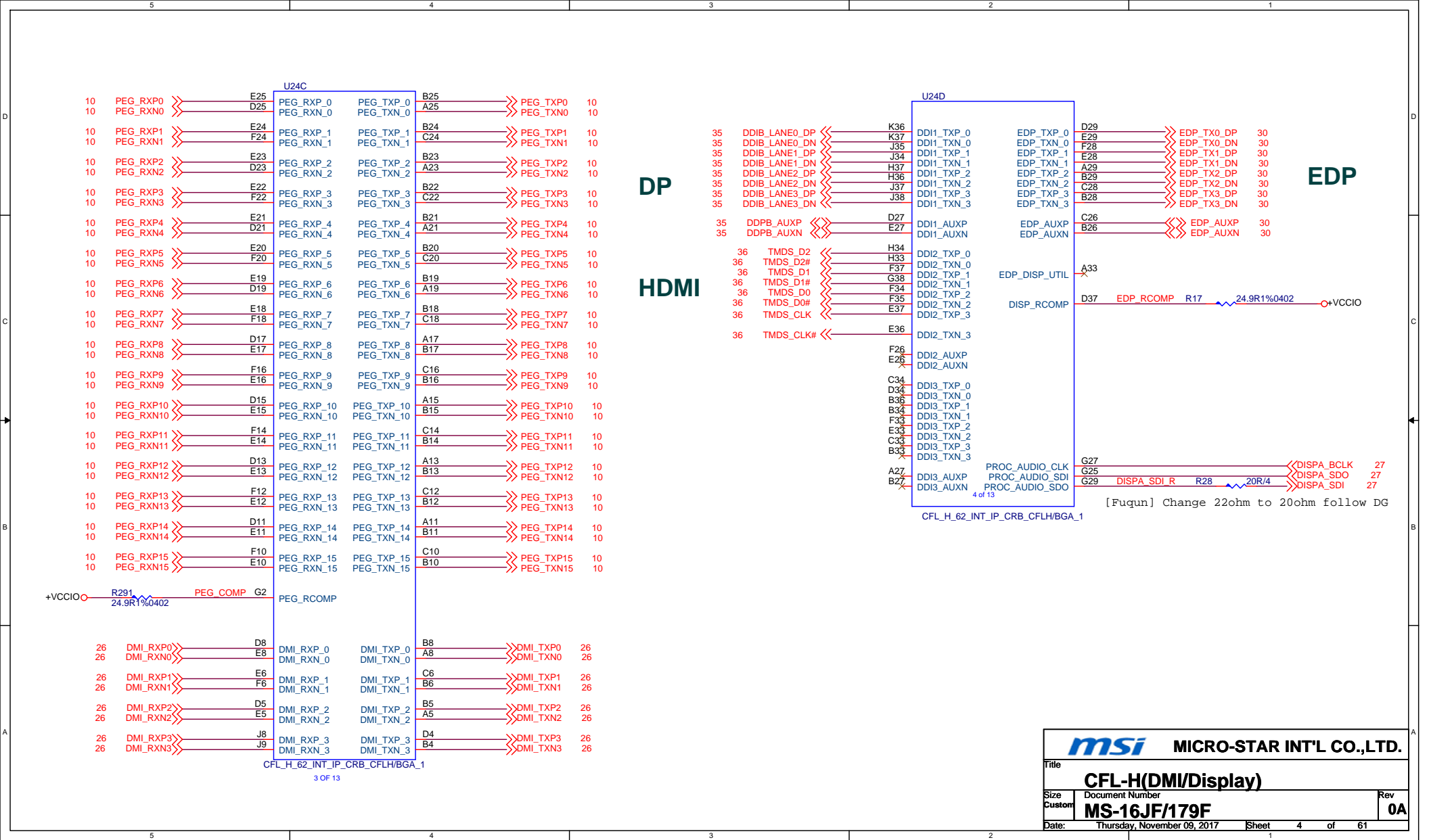
VCCST_PWRGD (Level Shifter 3.3V to 1.05V)

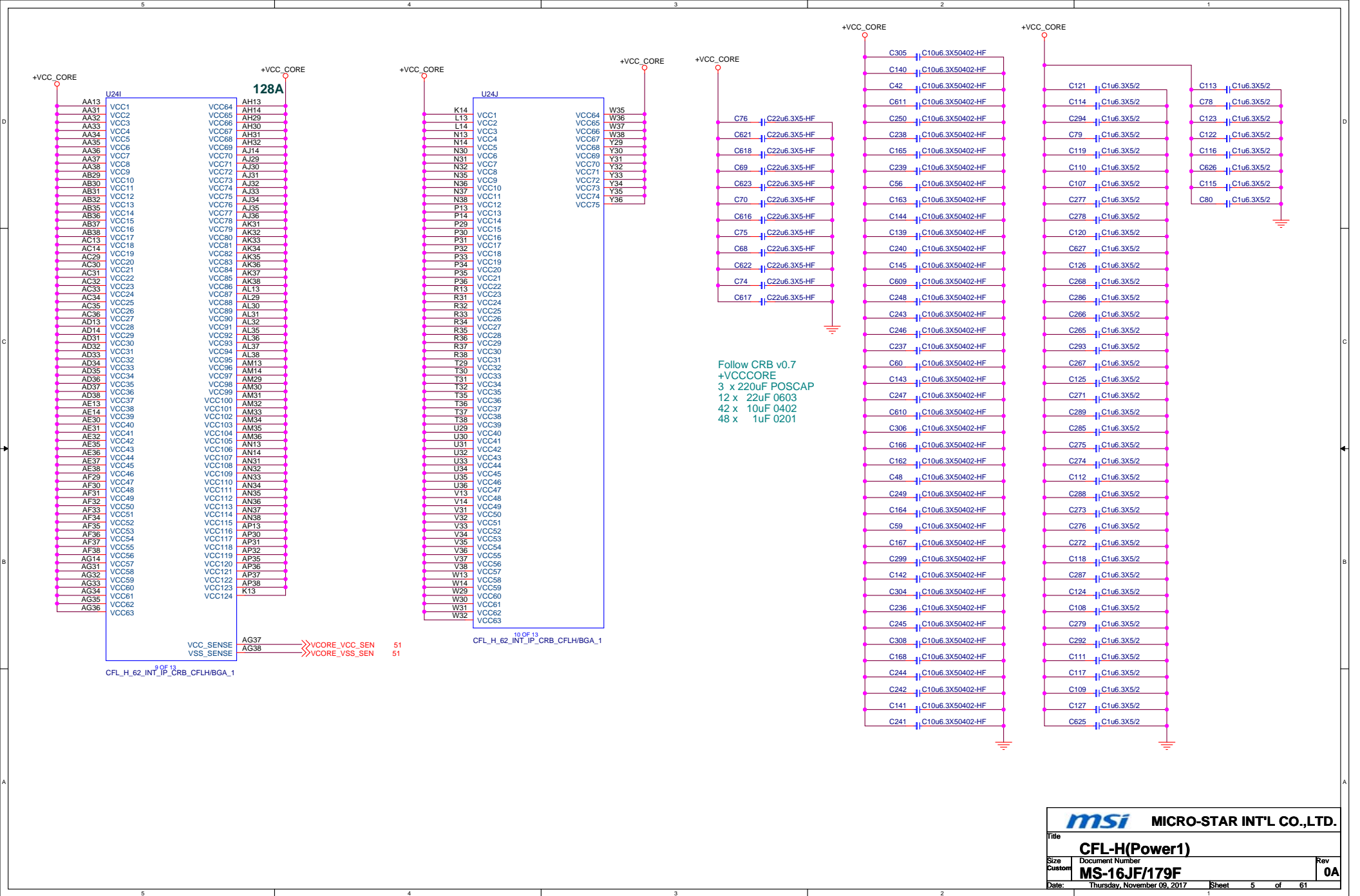


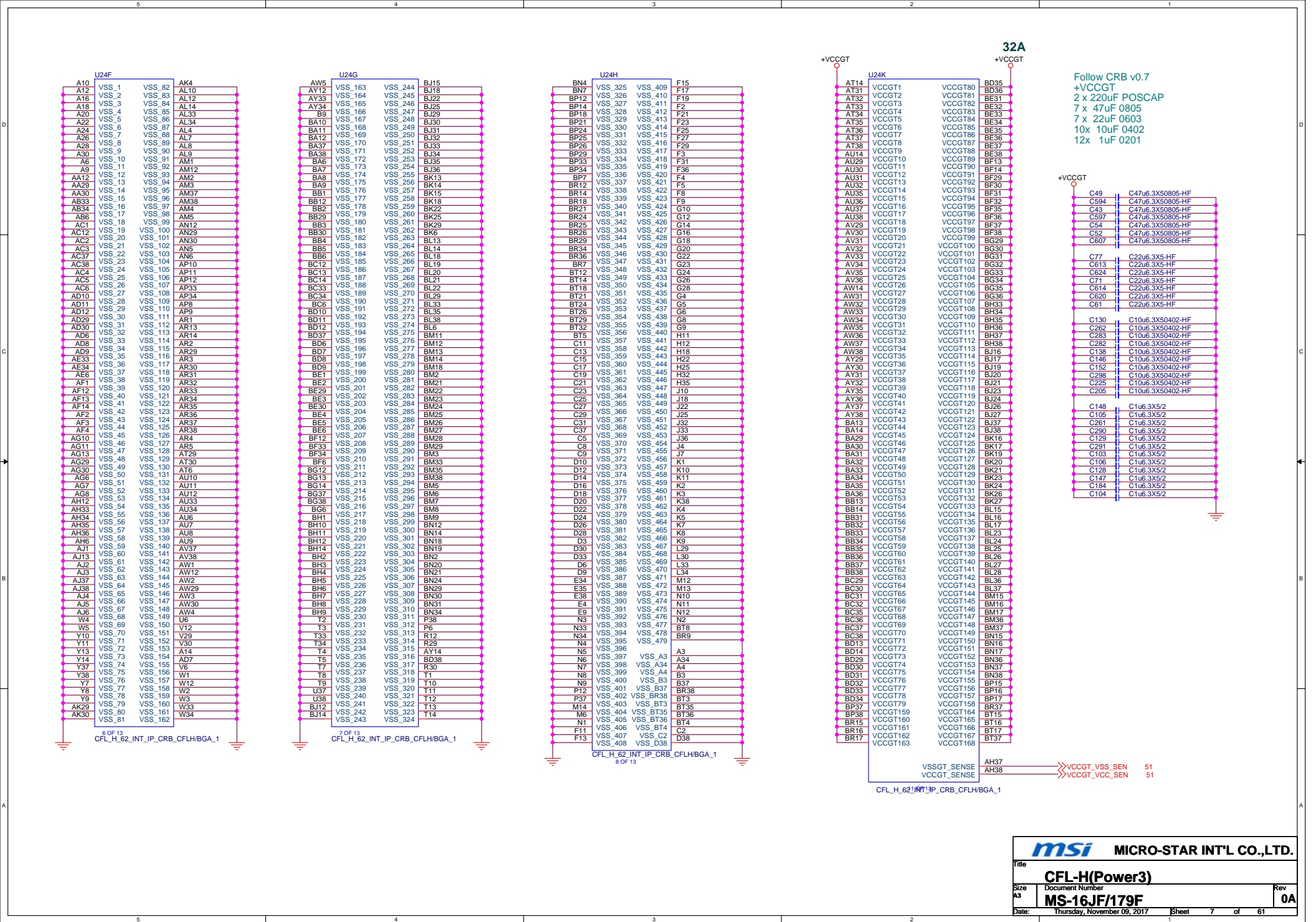
msi MICRO-STAR INT'L CO.,LTD.		
Title CFL-H(HOST)		
Size Custom	Document Number MS-16JF/179F	Rev 0A
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DDR Channel B

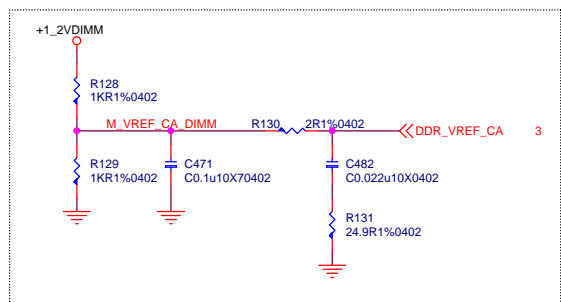
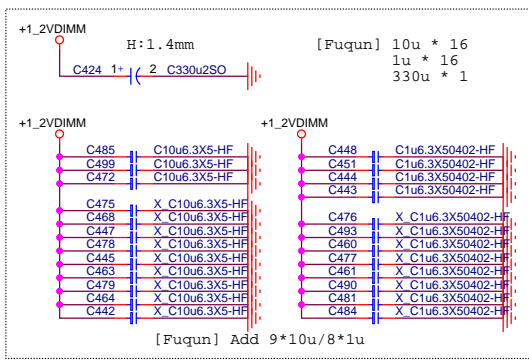
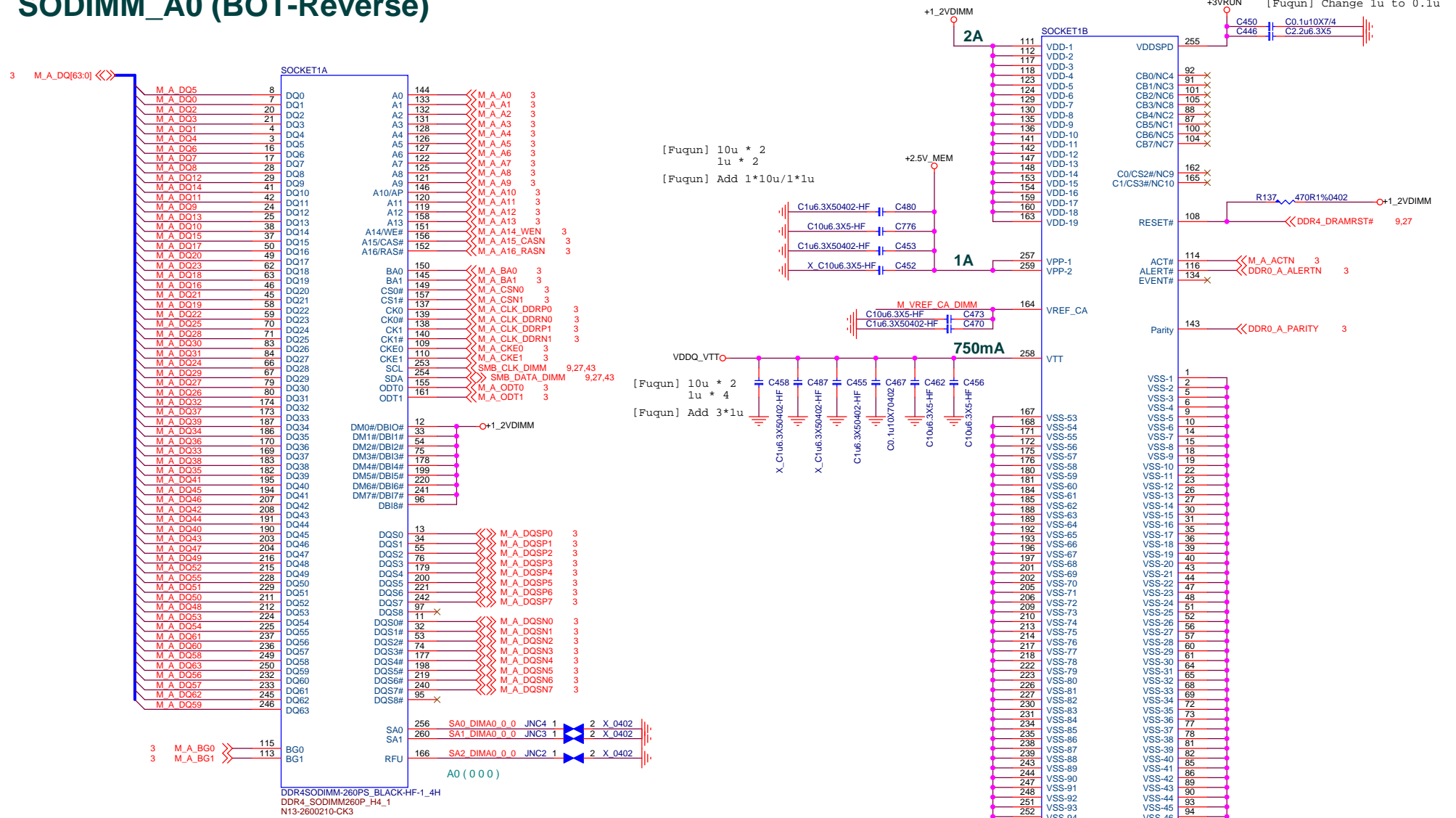




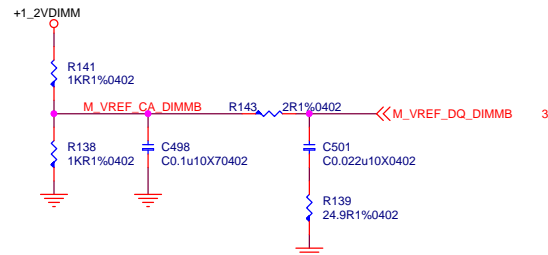
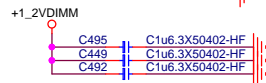
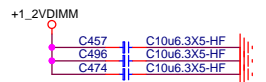
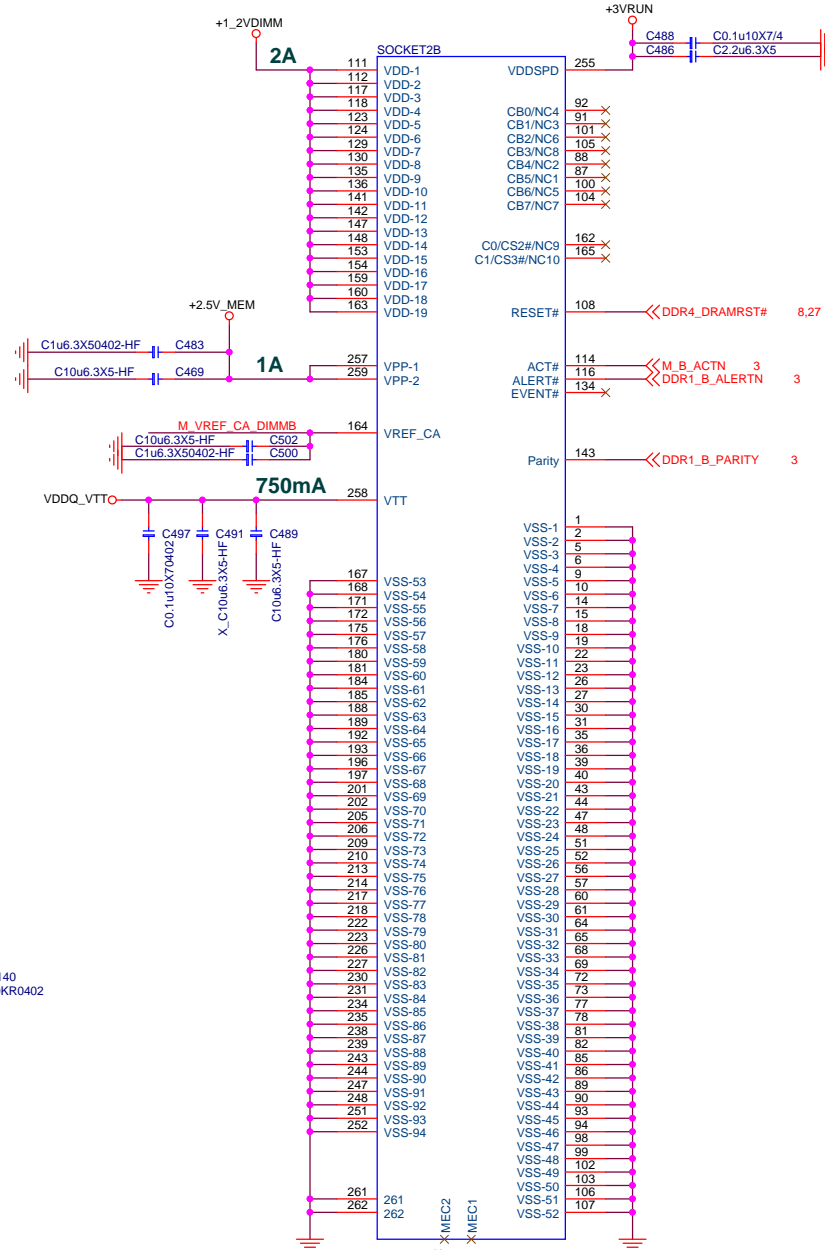
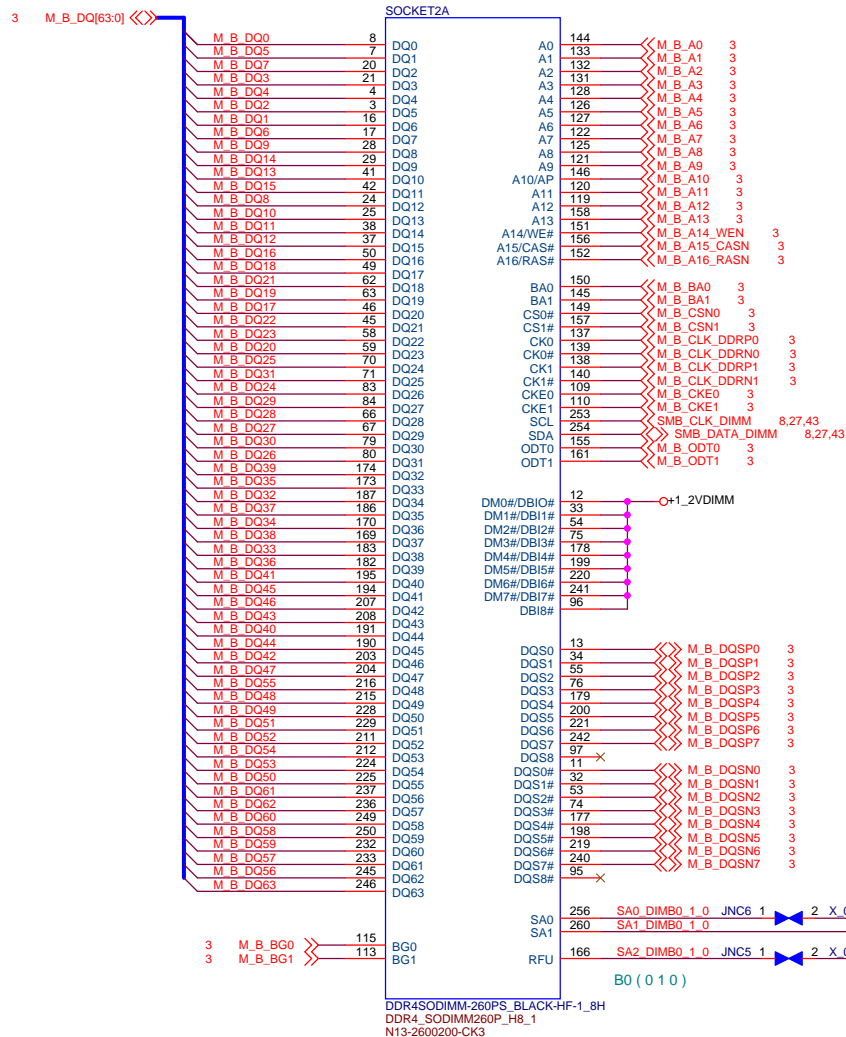




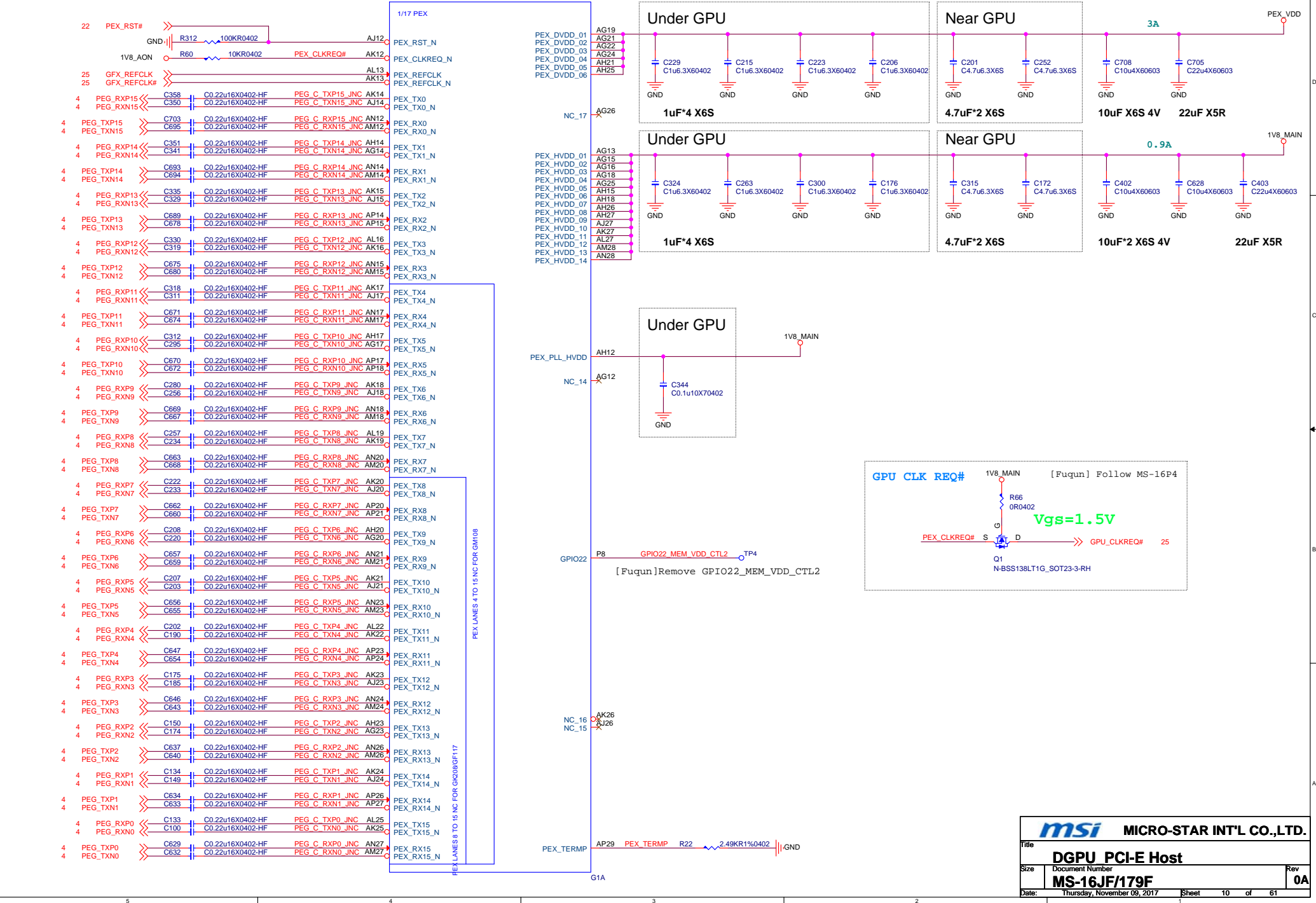
SODIMM_A0 (BOT-Reverse)



SODIMM_B0 (BOT-Reverse)

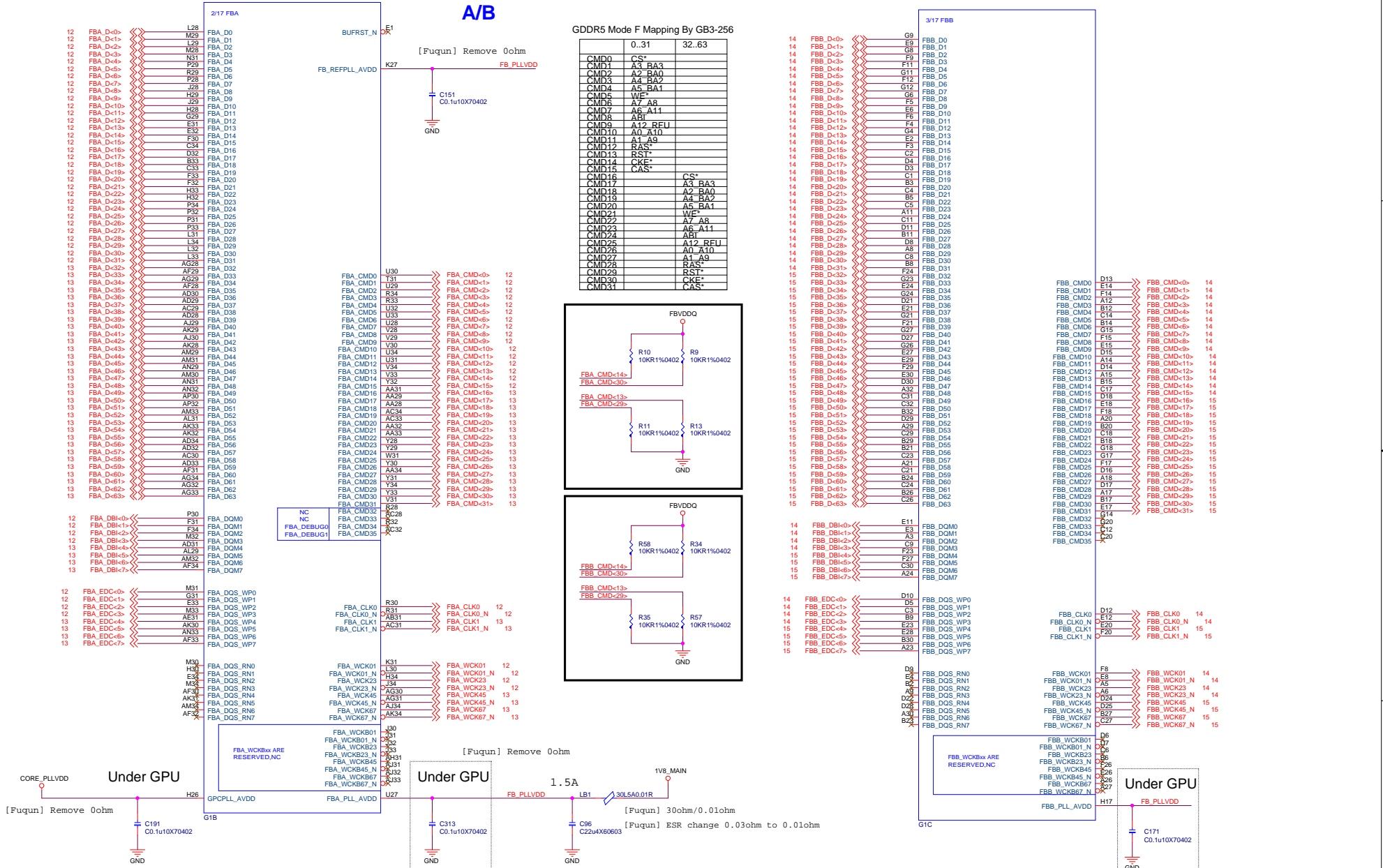


GPU PCI EXPRESS

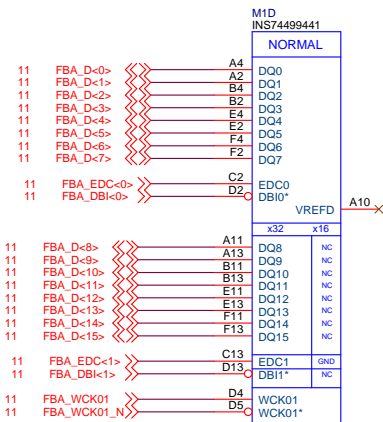


GPU Frame Buffer Partition A/B

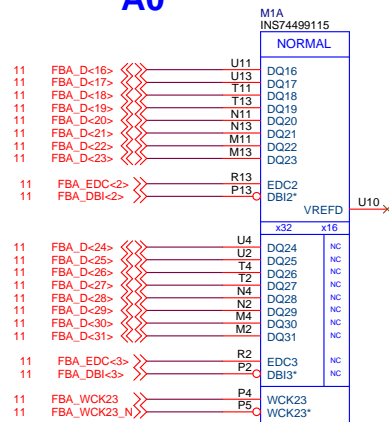
GDDR5 Mode F Mapping By GB3-256



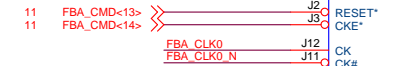
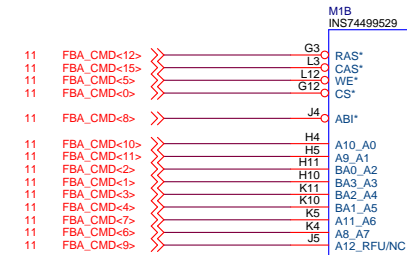
DGPU_GDDR5 FrameBuffer A0



K4G80325FB-HC28

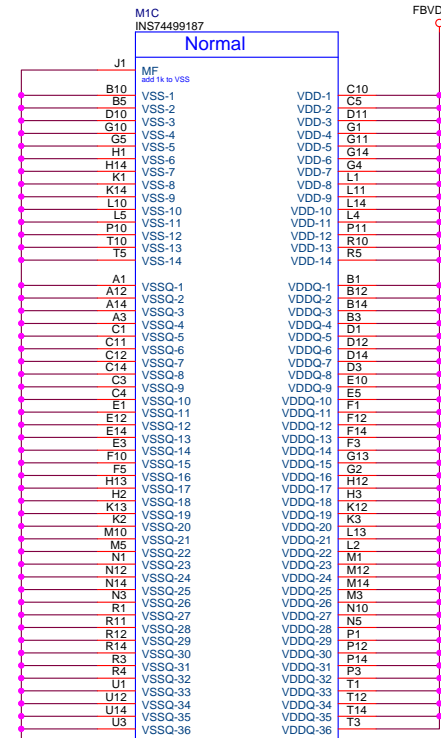
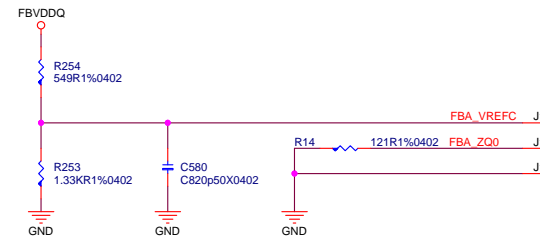


K4G80325FB-HC28

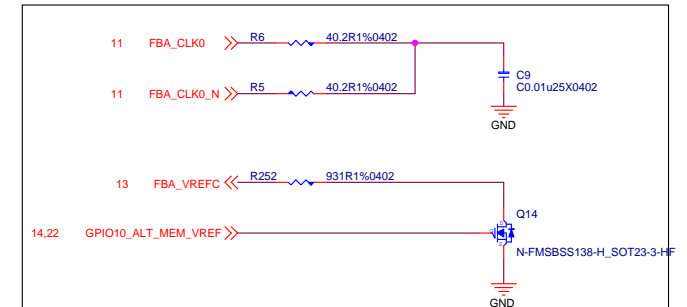
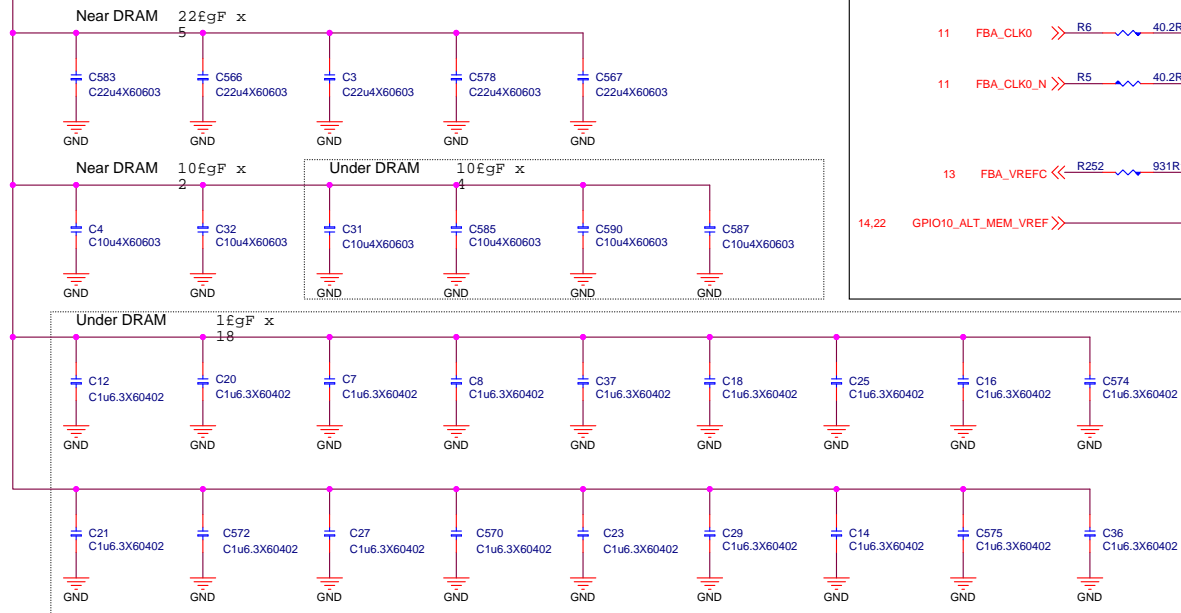


VPP_NC
VPP/NC

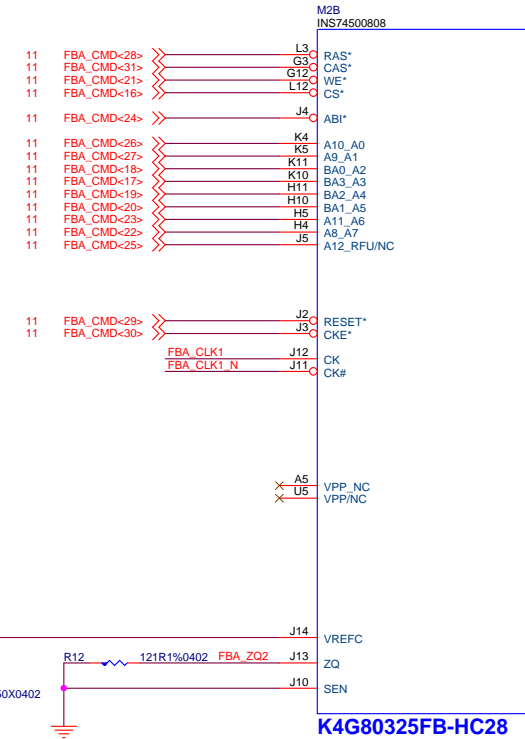
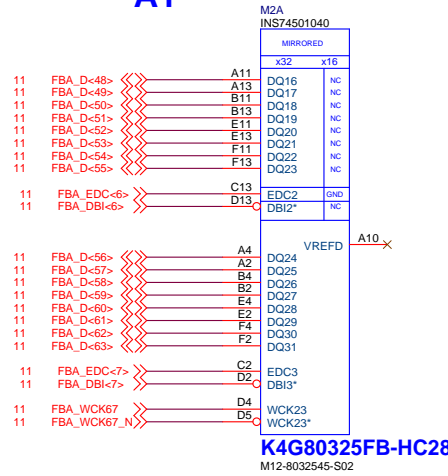
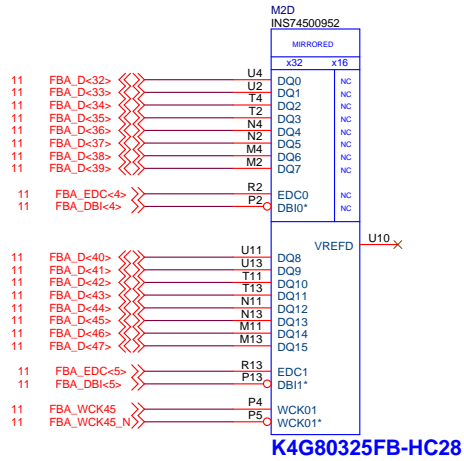
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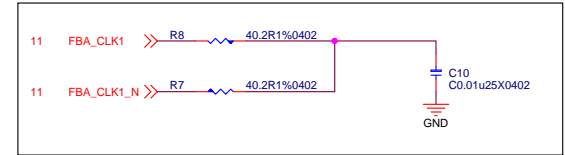
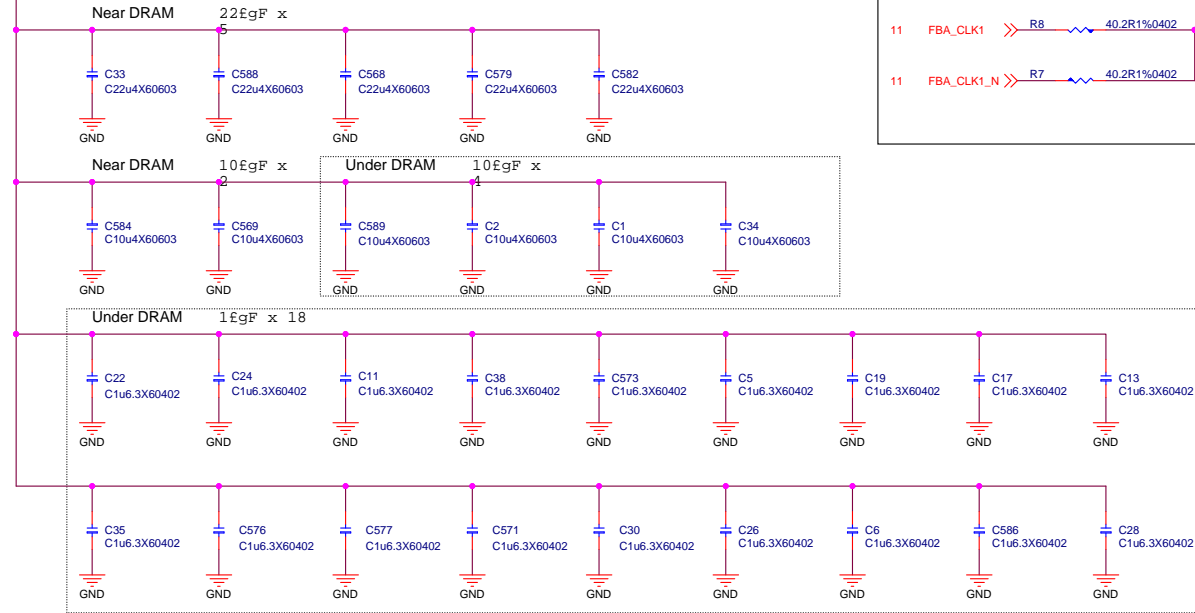
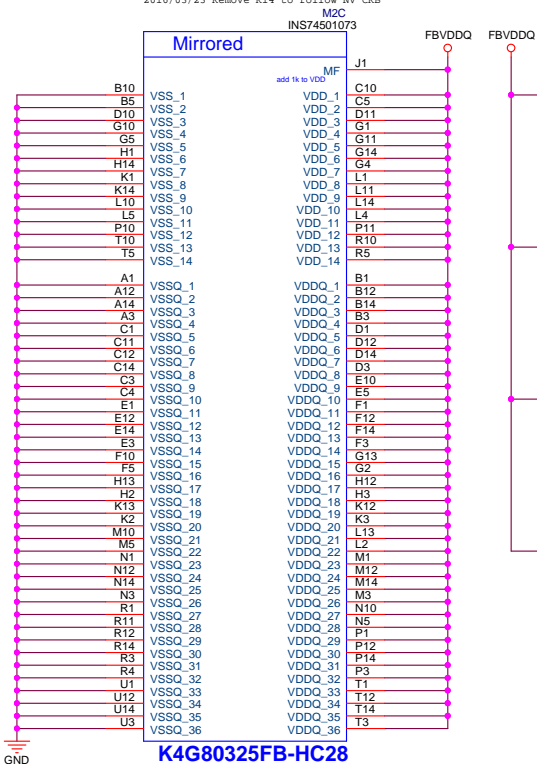
K4G80325FB-HC28



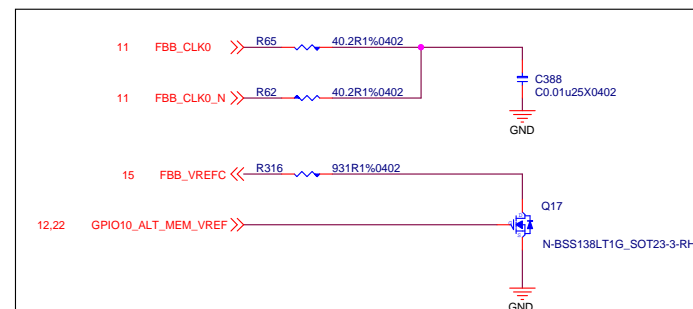
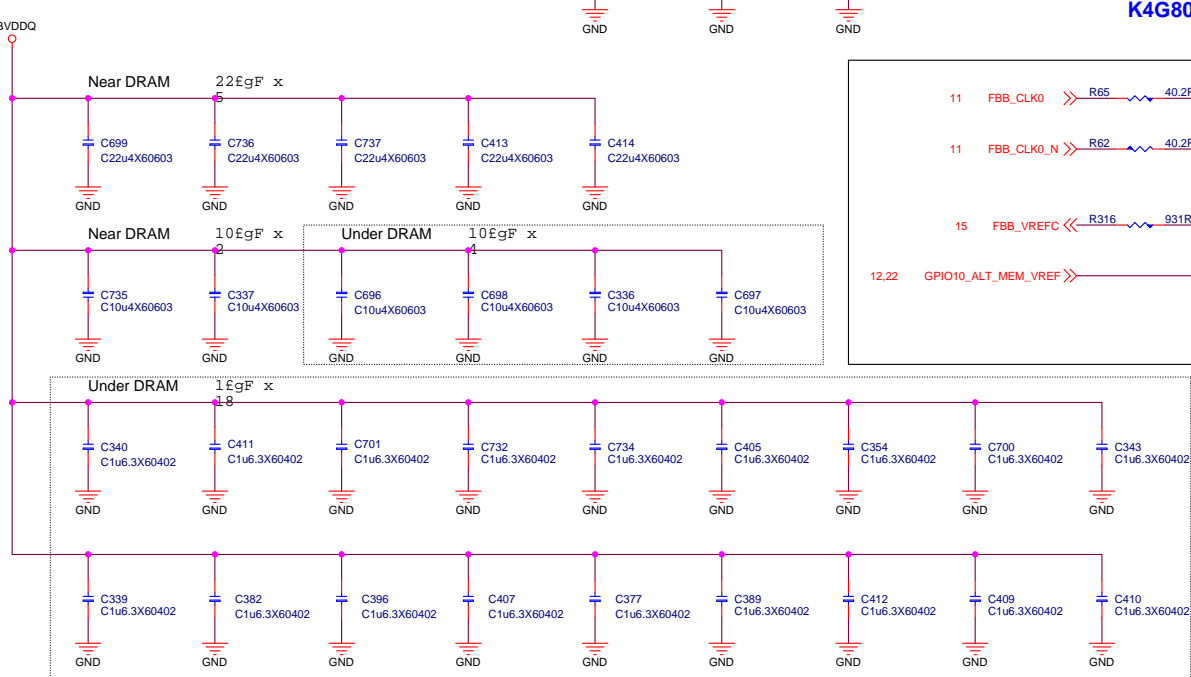
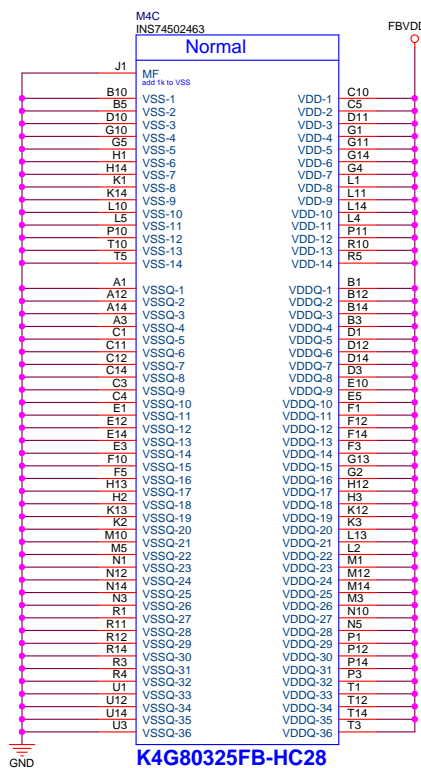
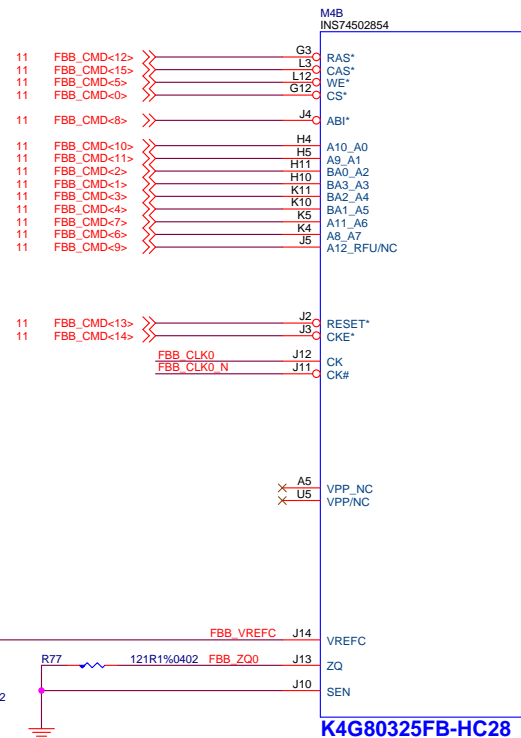
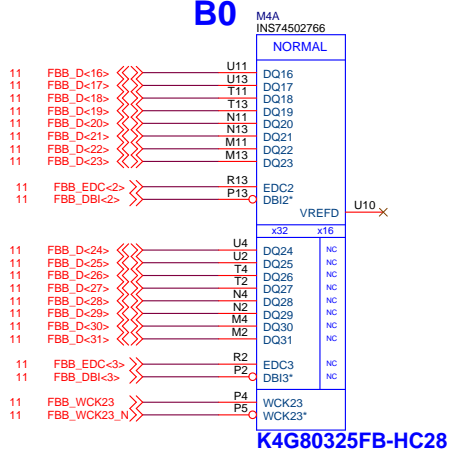
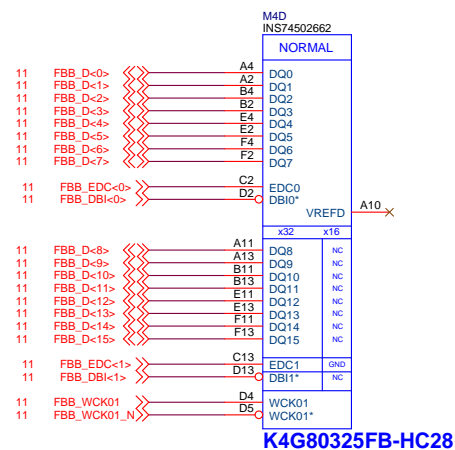
DGPU_GDDR5 FrameBuffer A1



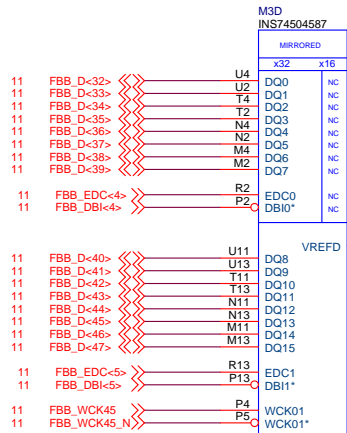
2016/03/23 Remove R14 to follow MV CRB



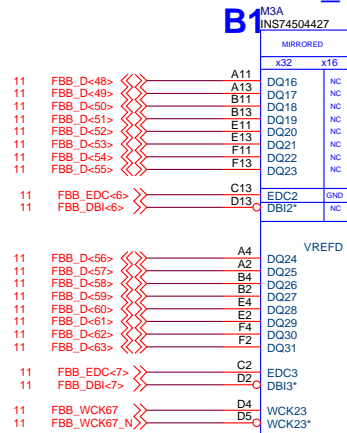
DGPU_GDDR5 FrameBuffer B0



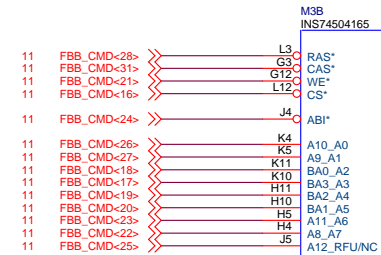
DGPU_GDDR5 FrameBuffer B1



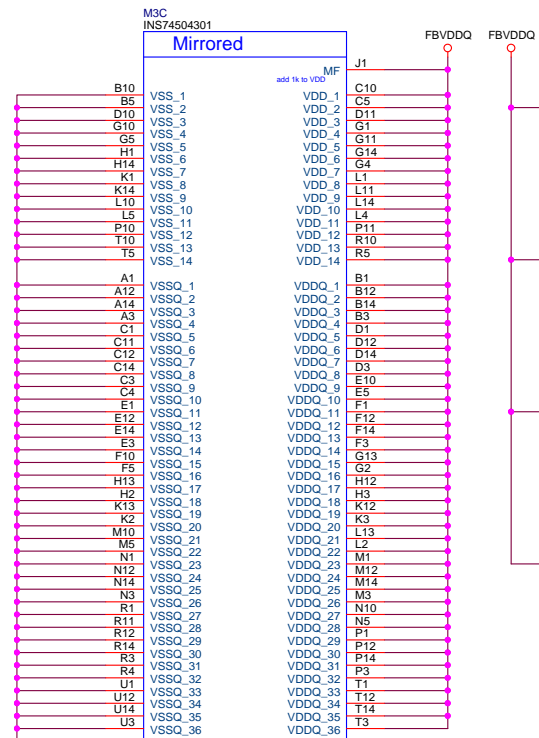
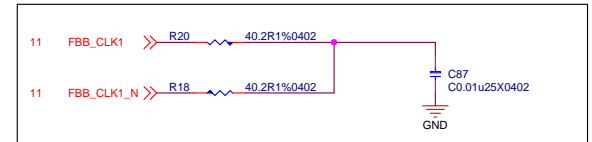
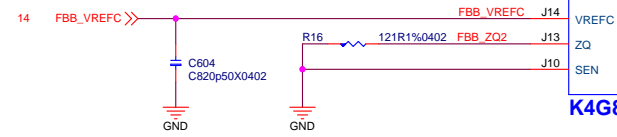
K4G80325FB-HC28



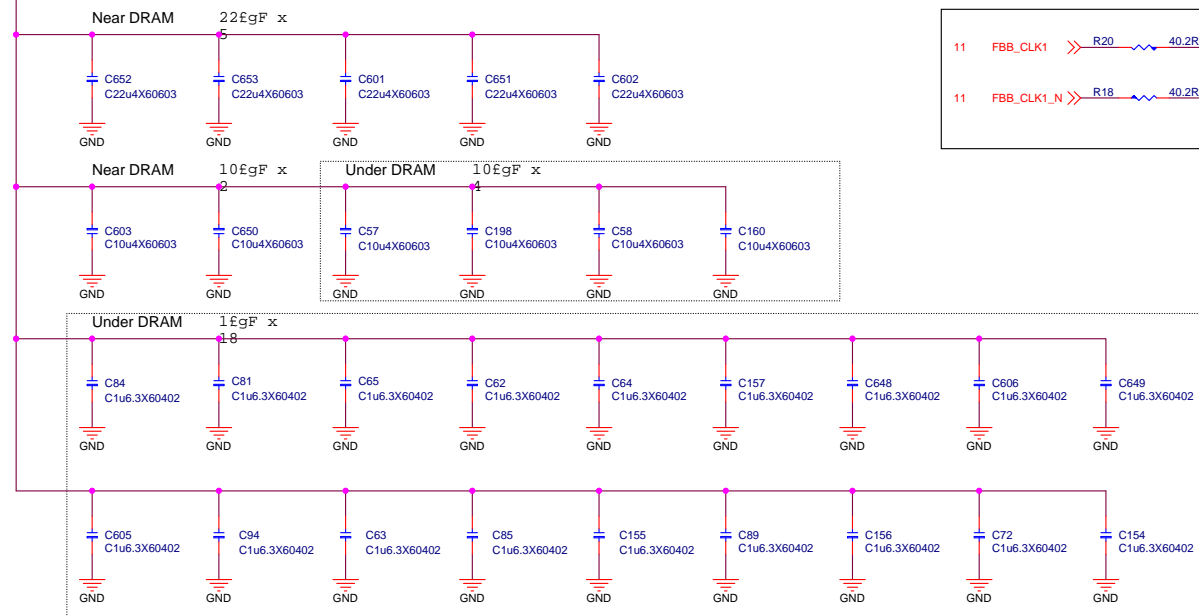
K4G80325FB-HC28



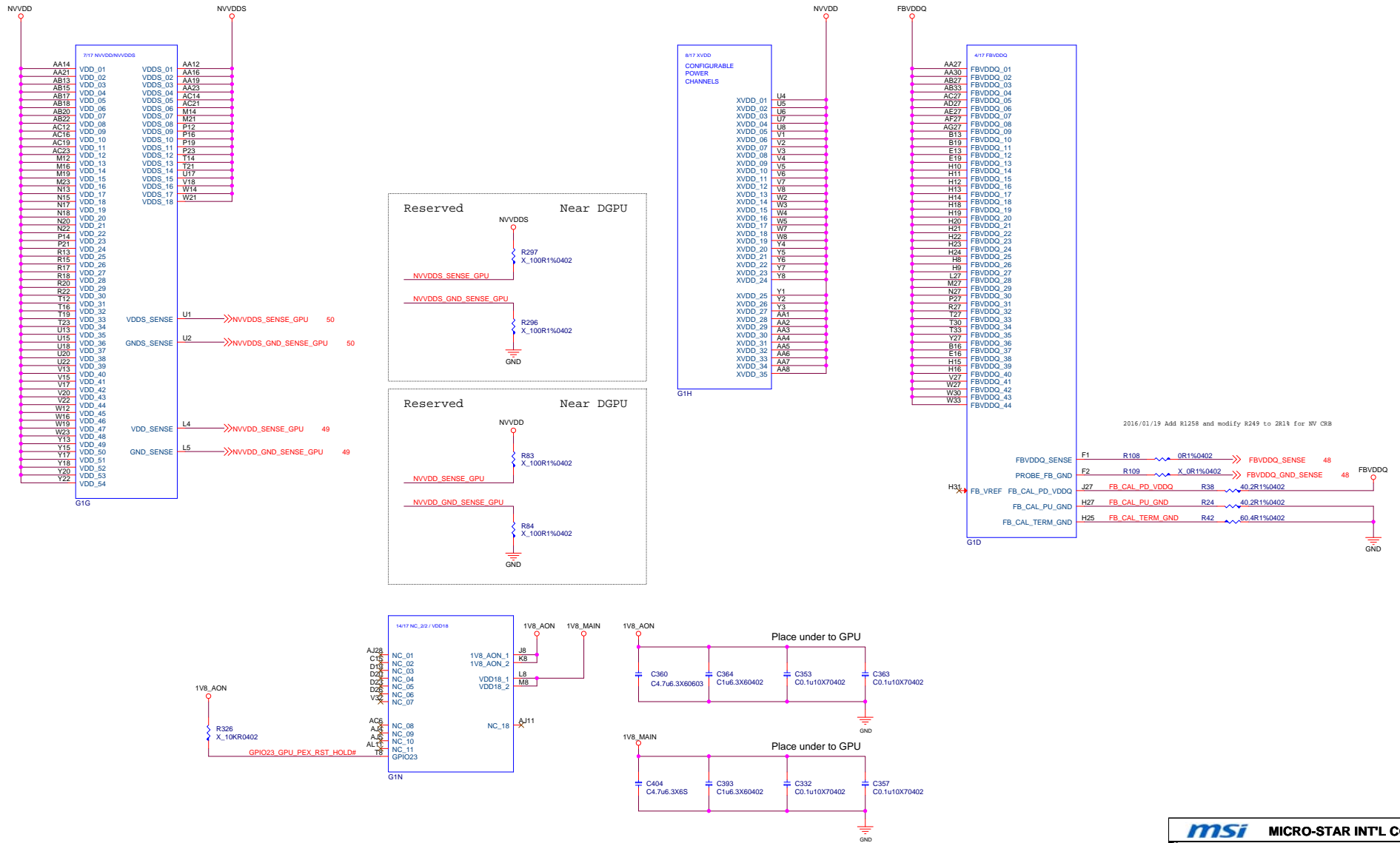
K4G80325FB-HC28



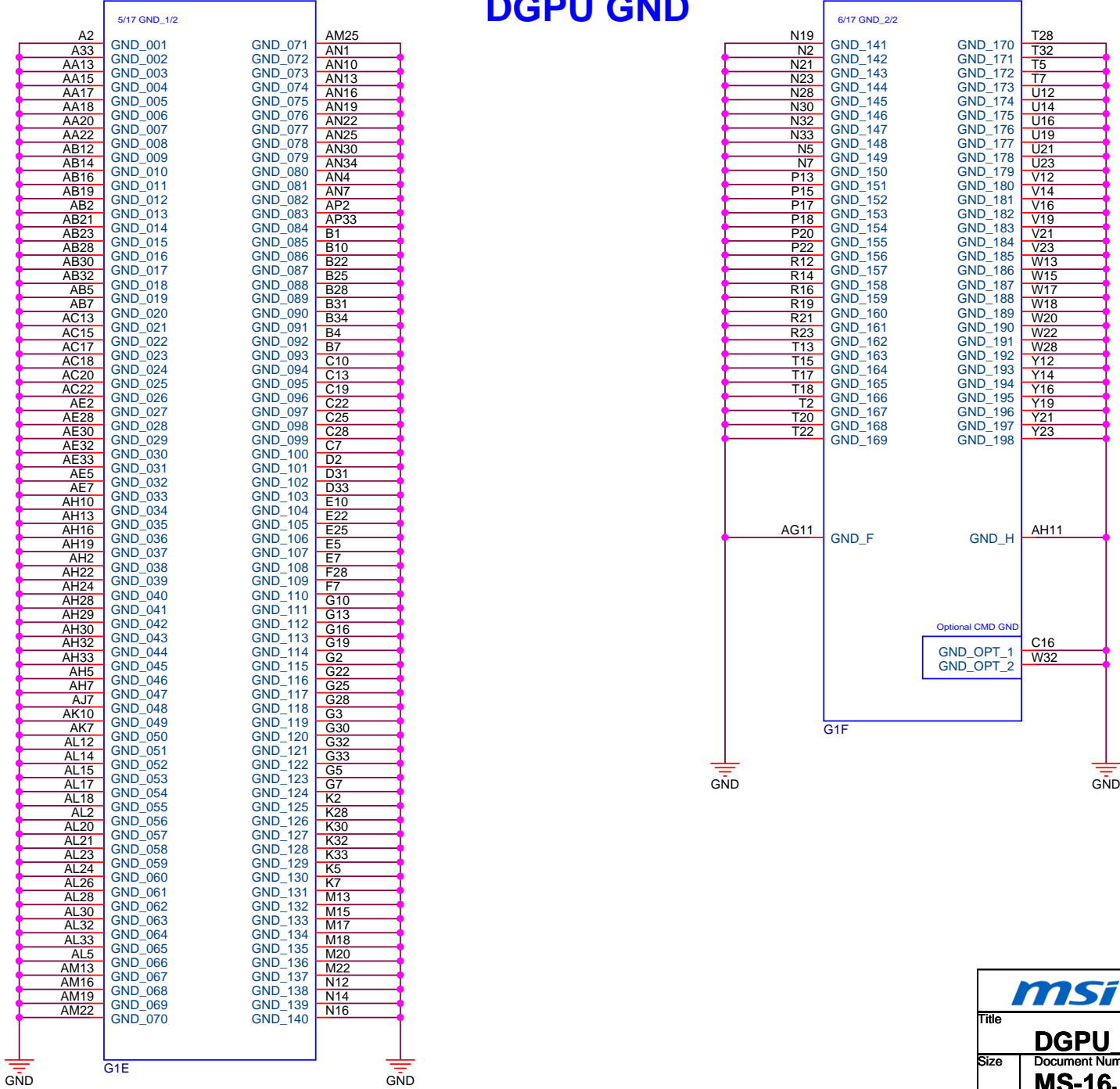
K4G80325FB-HC28



GPU NVVDD, FBVDDQ

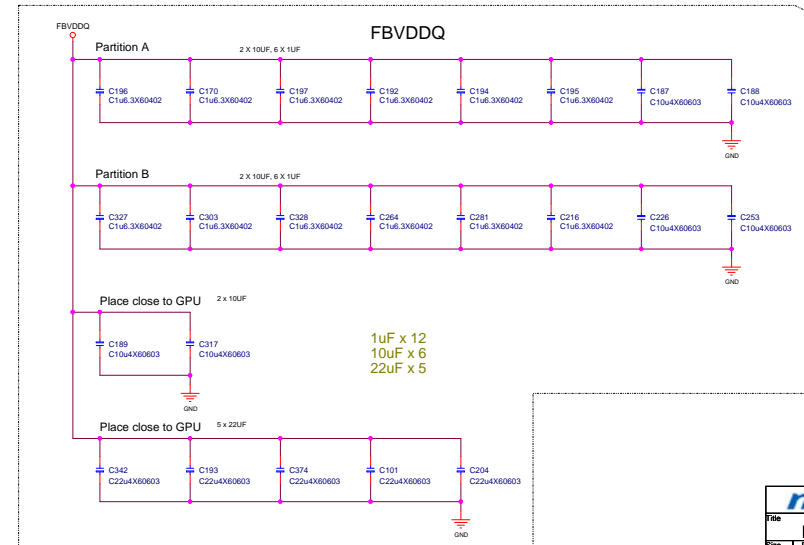
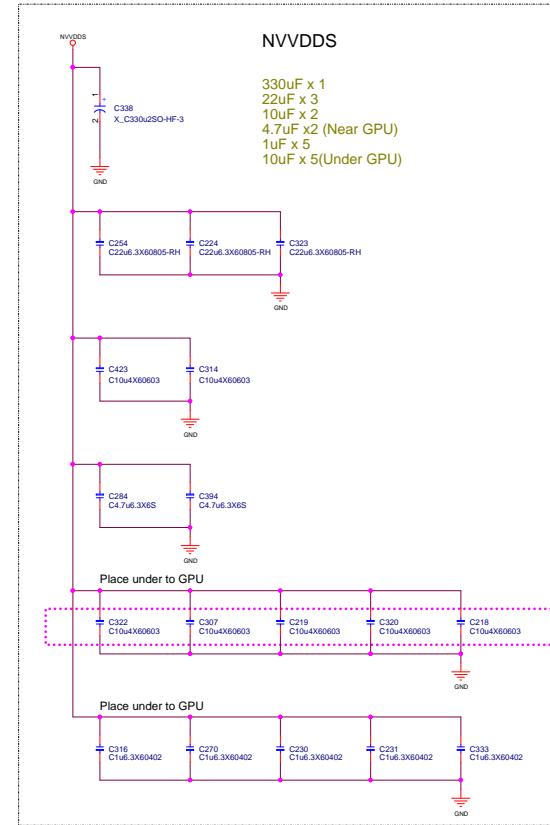
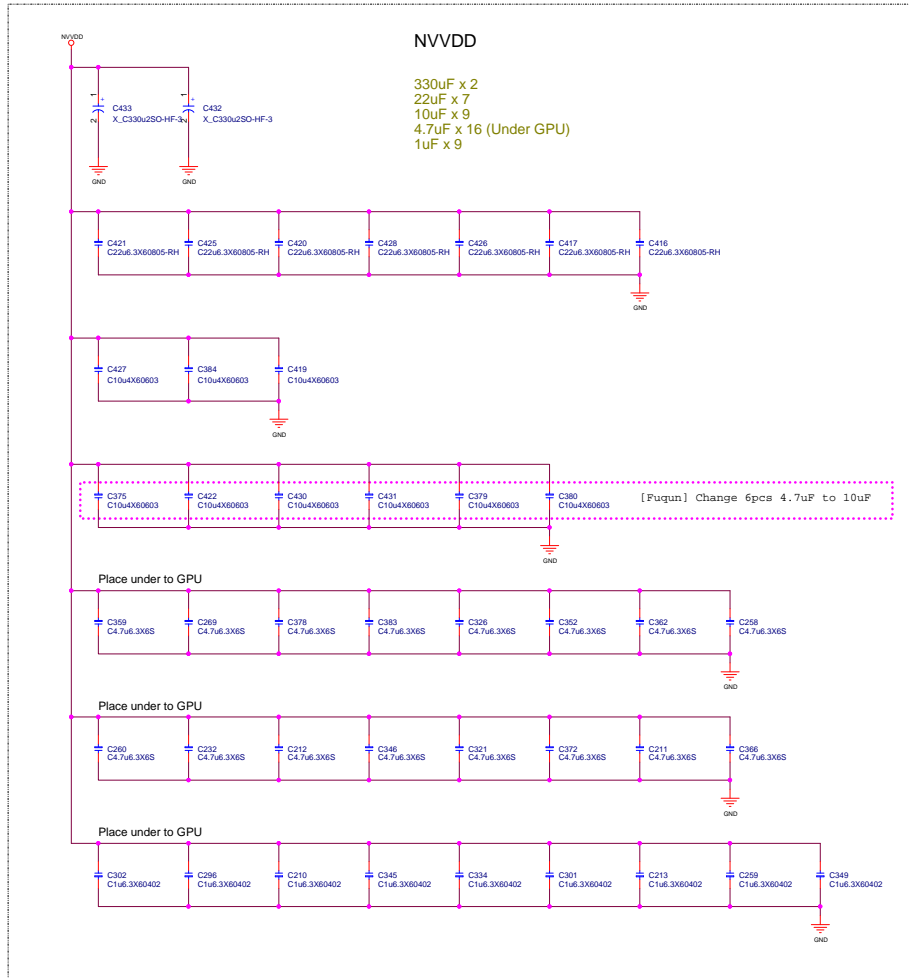


DGPU GND

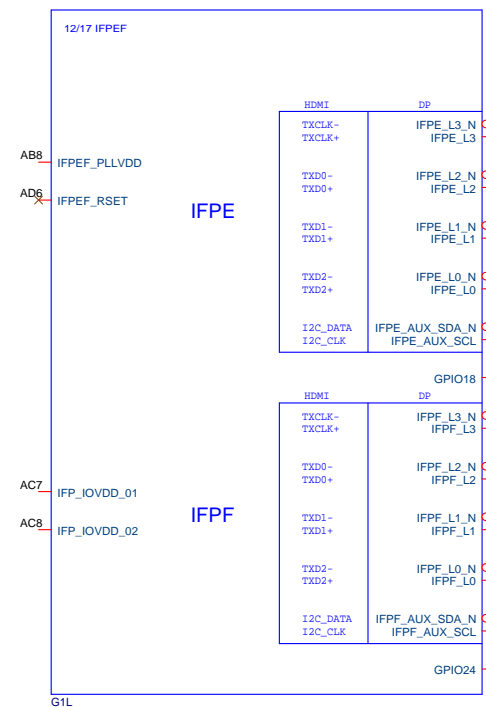
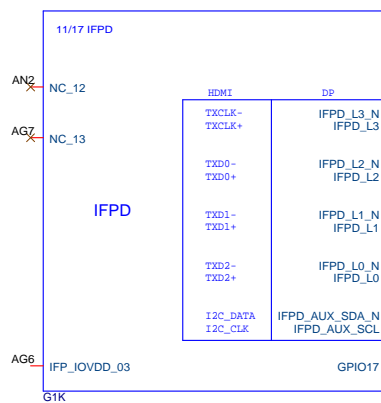
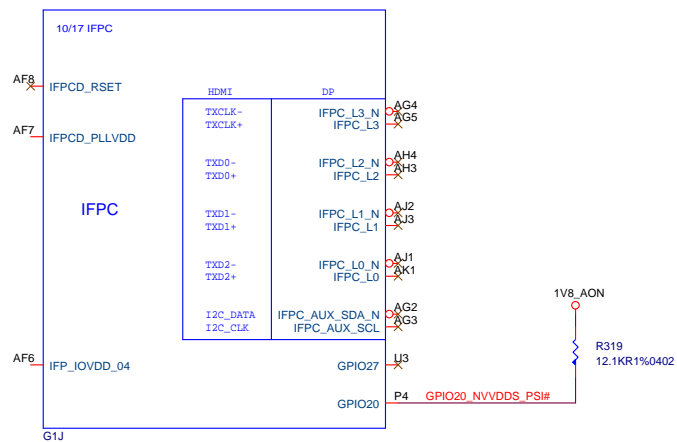
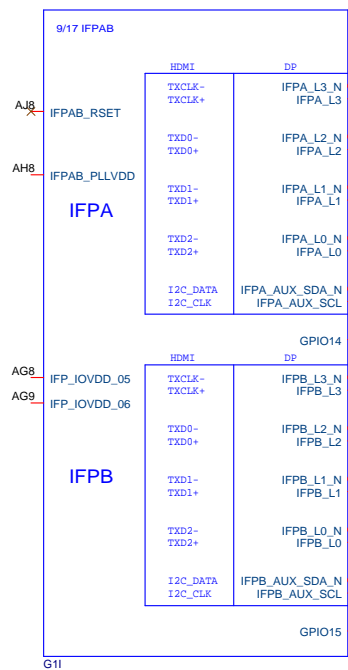


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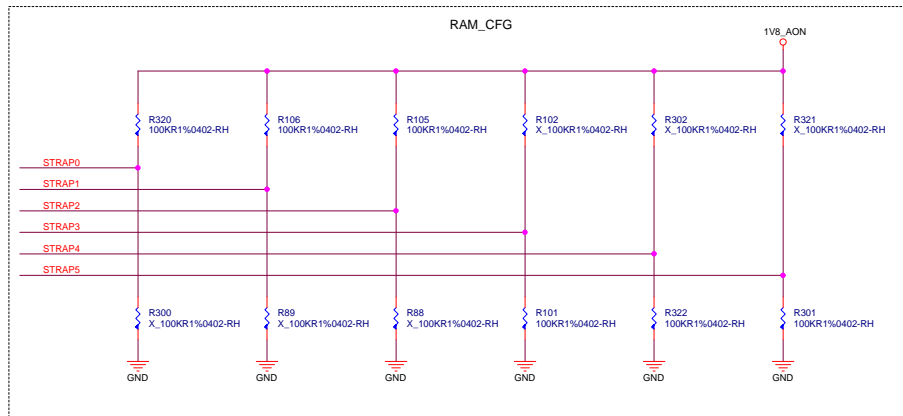
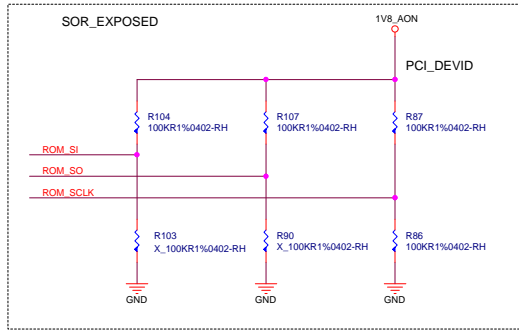
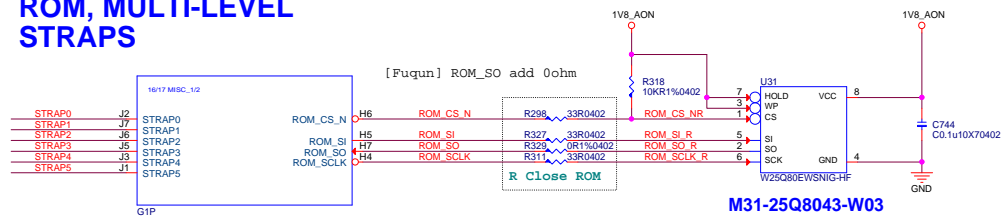
GPU DECOUPLING



DACA, Display IF

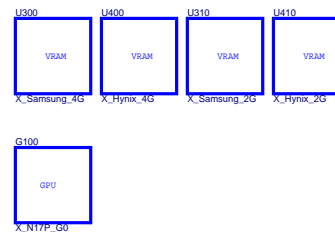


ROM, MULTI-LEVEL STRAPS



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	R330.R92.R91
L	L	H	0x1 Micron: MT51J256M32HF-70:A	R354.R92.R91
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R330.R106.R91
L	H	H		
H	L	L		
H	L	H		
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R330.R106.R105
H	H	H	0x7 Samsung: M12-41325A5-S02 / K4G41325FE-HC28	R354.R106.R105
L	L	M	0x8 Micron: EDW032BABG-70-F:A	R330.R354.R92.R91
L	M	L		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

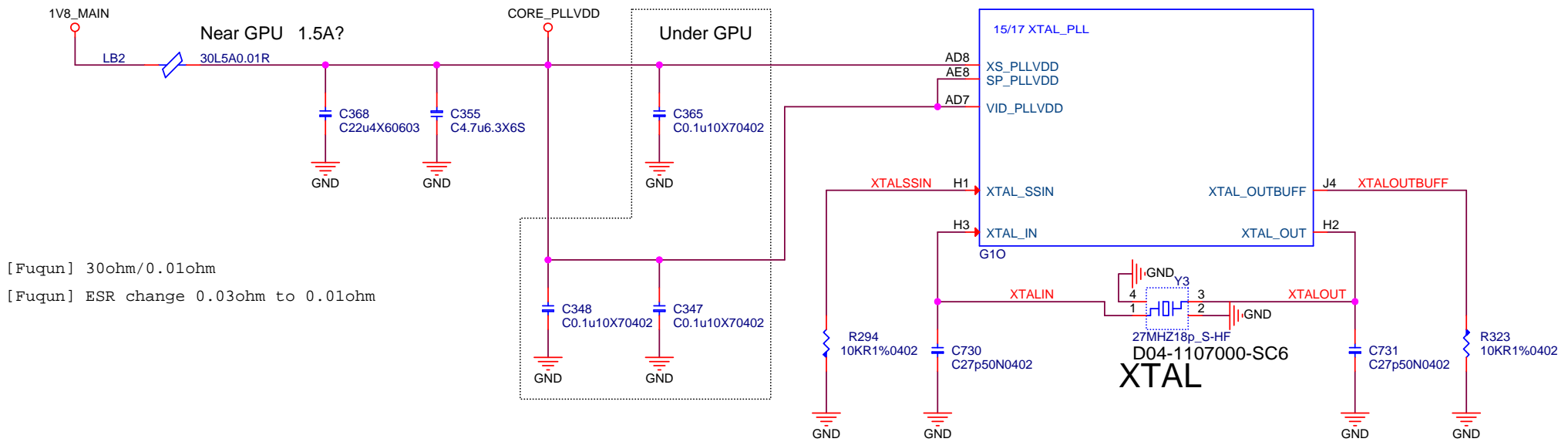
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

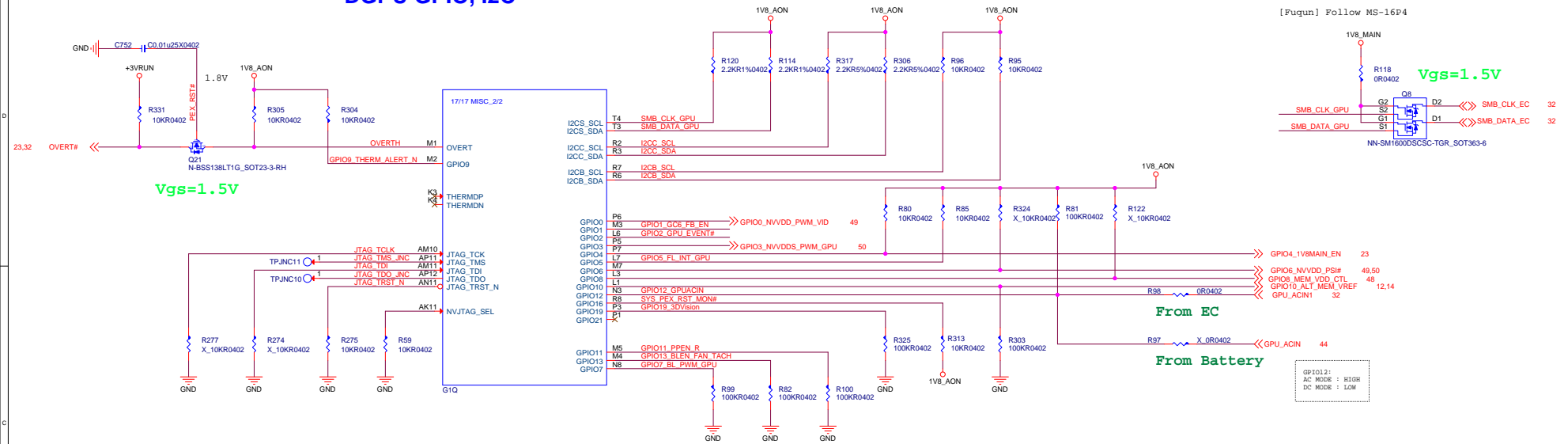
DGPU XTAL



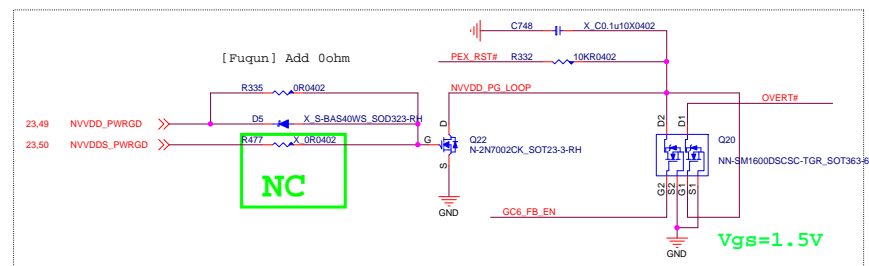
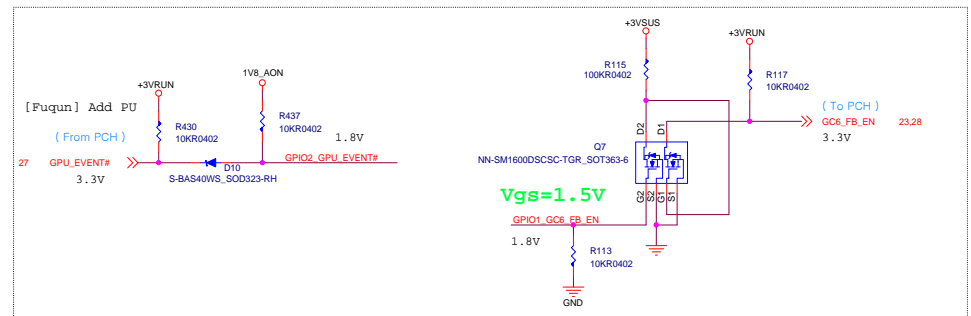
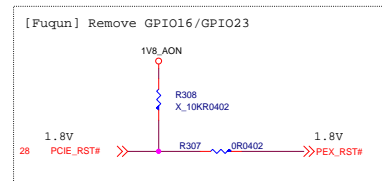
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DGPU XTAL		
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DGPU GPIO, I2C



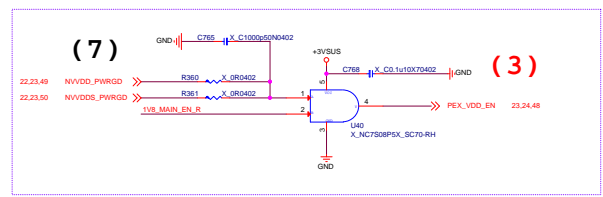
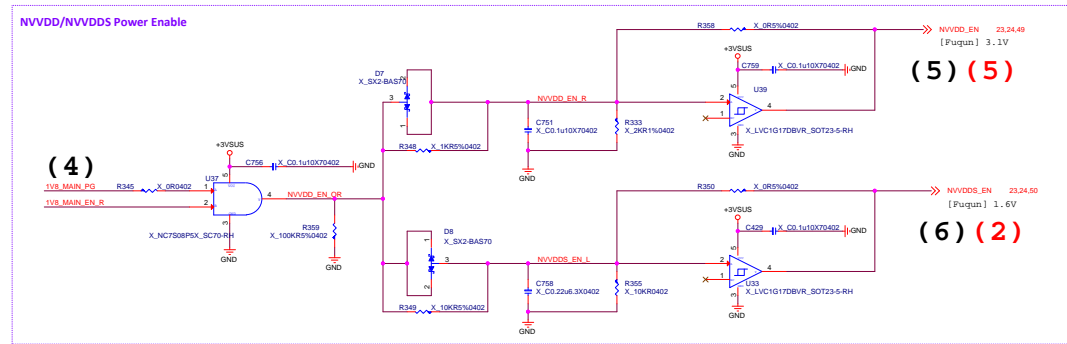
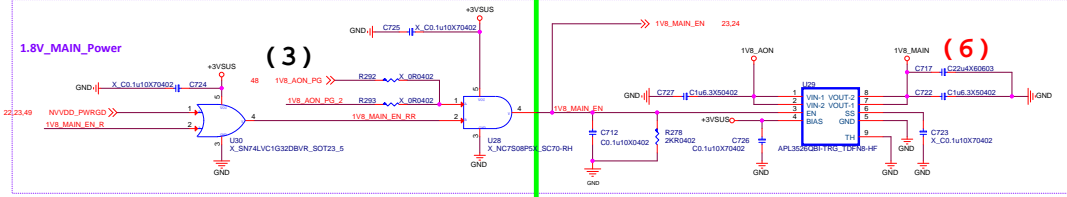
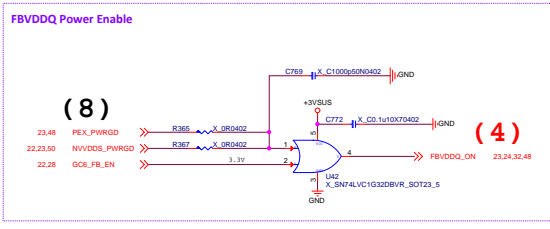
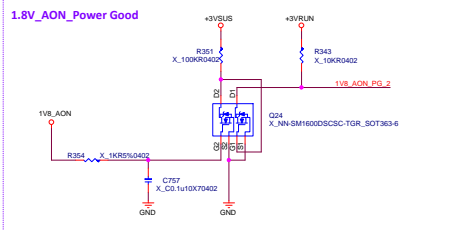
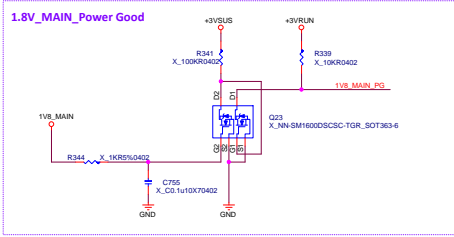
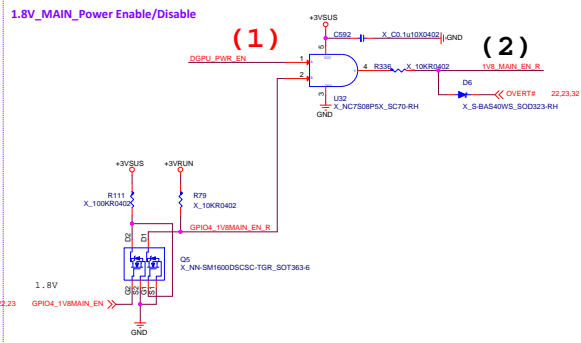
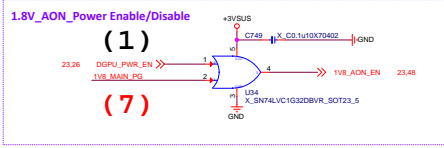
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to V18 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to V18 _AON
GPIO3	NVVD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to V18 output
GPIO4	V18_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to V18 _AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, V18 pull-up to V18 _AON
GPIO6	NVVD_PSI	O	Phase shedding	10K pull-up to V18 _AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to V18_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to V18_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IPFA	
GPIO15	HPD_B	I	Hot Plug Detect for IPFB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to V18 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IPFD	
GPIO18	HPD_E	I	Hot Plug Detect for IPFE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IPFC	



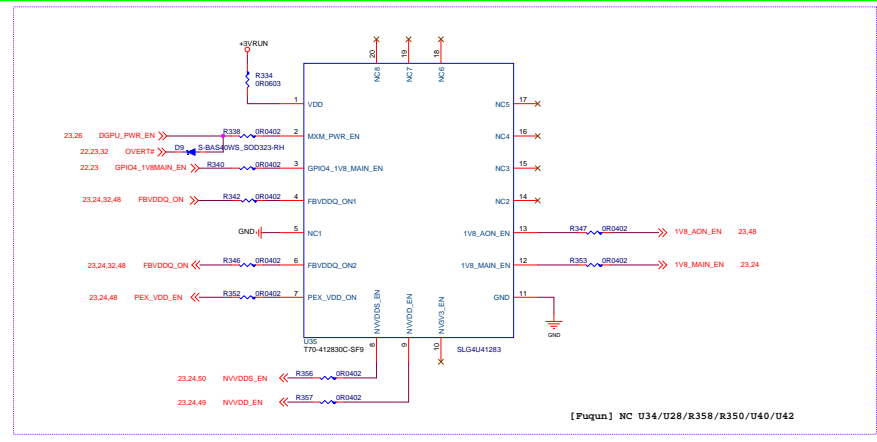
nVIDIA Power Sequence Control

Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV/NVDD -> NVDD/PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power Off=NVDD/PEX_VDD/FBVDDQ->NVDD->NV3V3->1V8_MAIN->1V8_AON

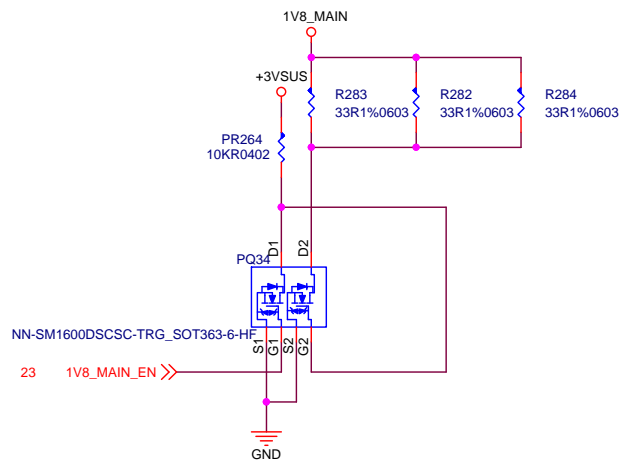
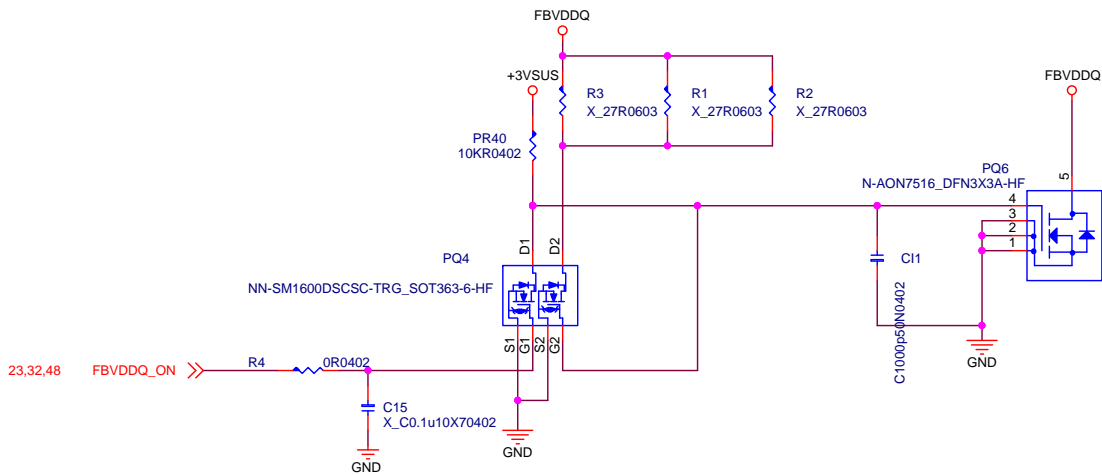
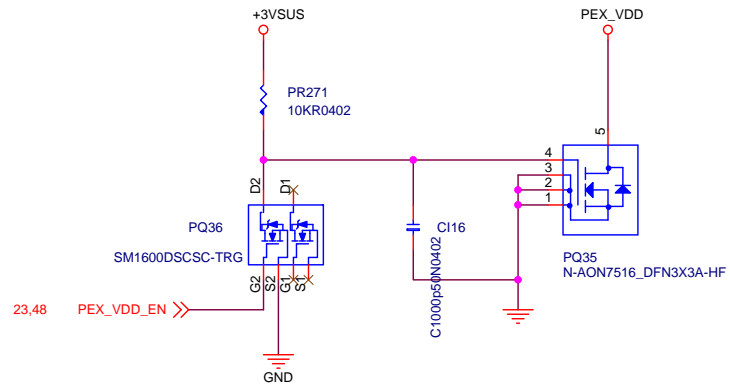
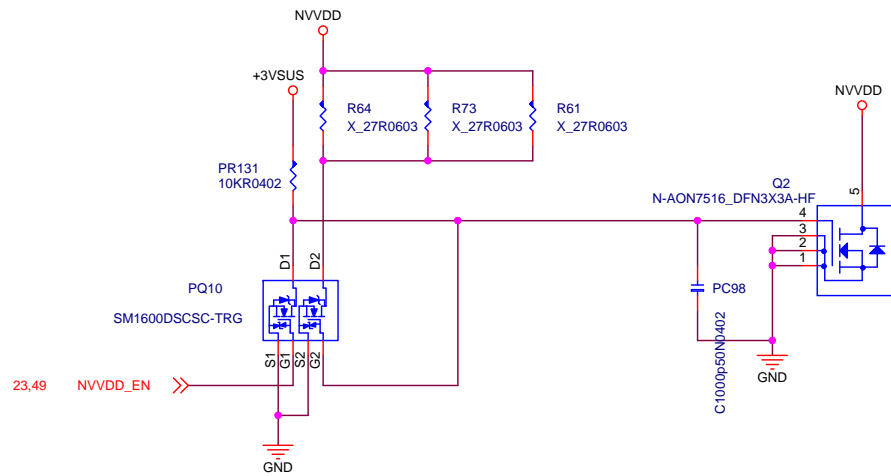
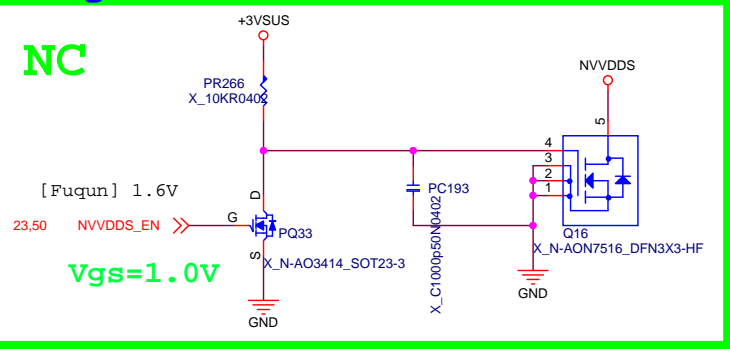


NC



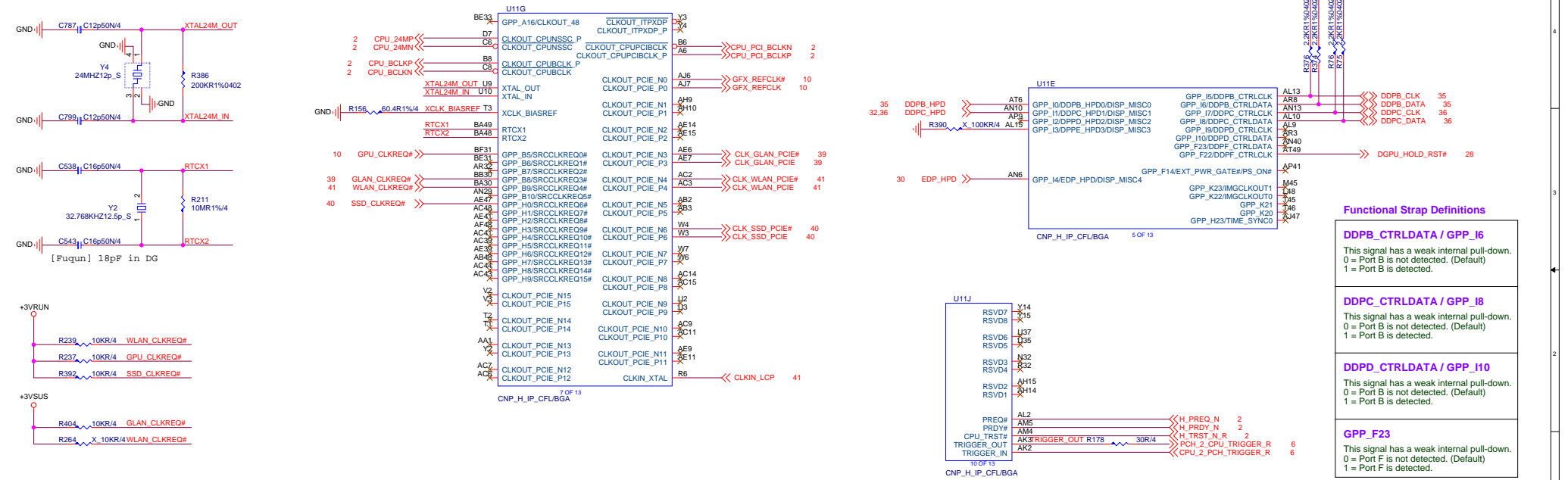
Discharge

NC



msi MICRO-STAR INT'L CO.,LTD.	
Title	
DGPU Discharge	
Size	Document Number
MS-16JF/179F	
Date:	Rev
	0A

HM370 (RTC/Clock)



HM370 (DMI/PCIE/USB3.1/USB2.0/CNV1)

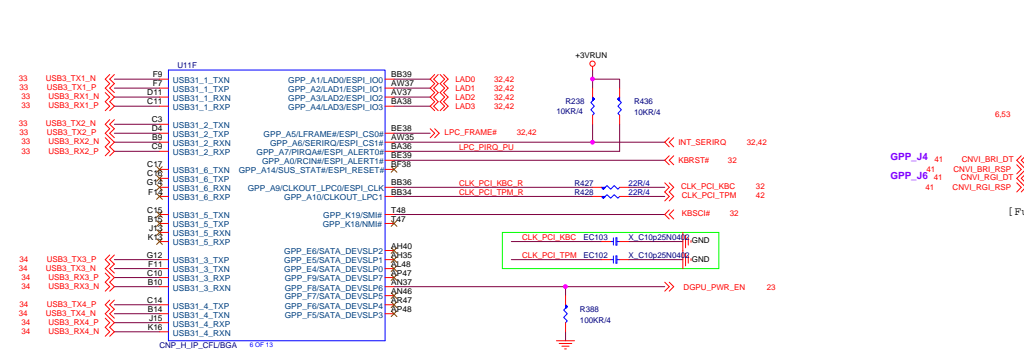
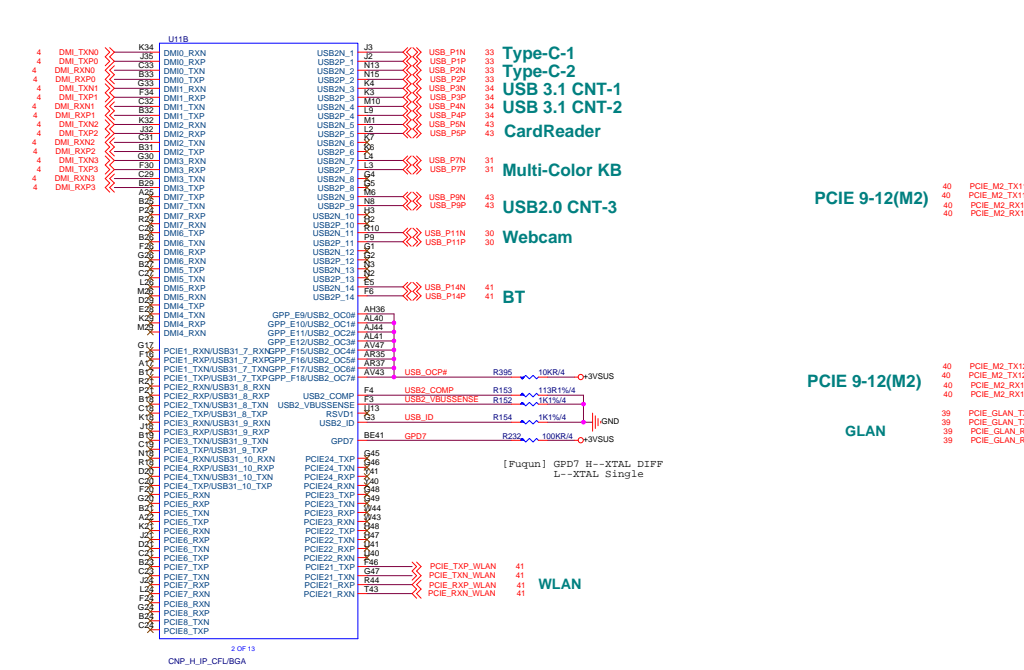


Diagram showing CNL PCH-H Preliminary HSIO Lane Assignments. The diagram includes a table of lane assignments for various components (LAN, HDD, WLAN, CardReader, M.2 SSD, AR(TBT)) and a table of component assignments for different SKUs (HM370, QM370, CH246).

Component	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
LAN																														
HDD																														
WLAN																														
CardReader																														
M.2 SSD																														
AR(TBT)																														

SKU	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030
HM370	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030
QM370	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030
CH246	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030

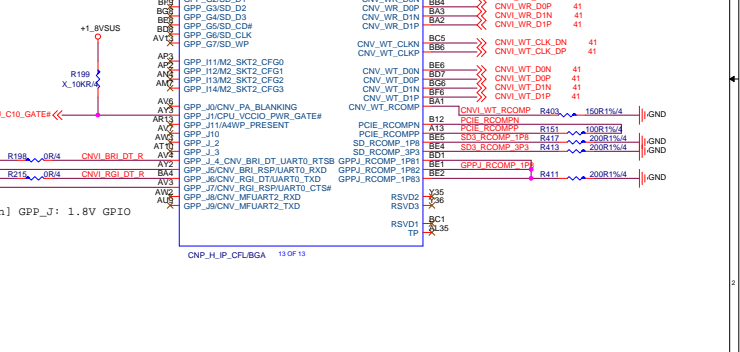
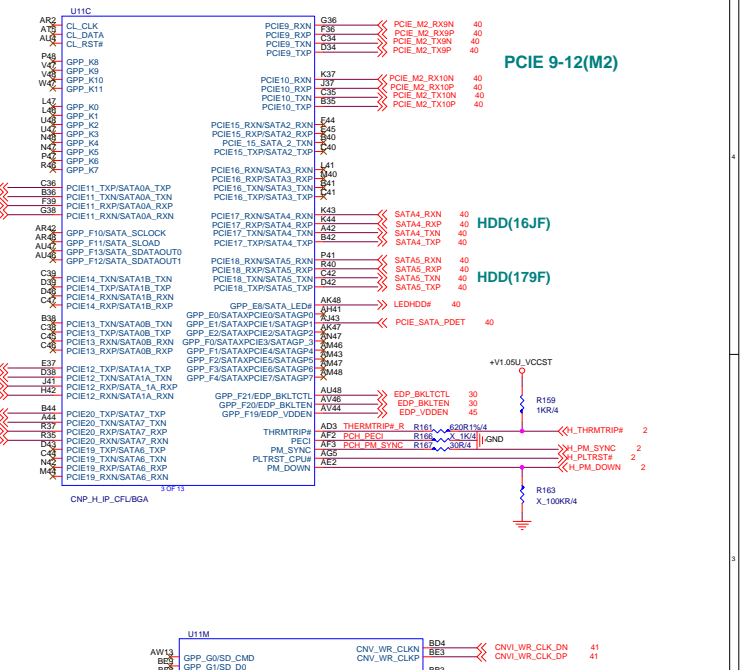


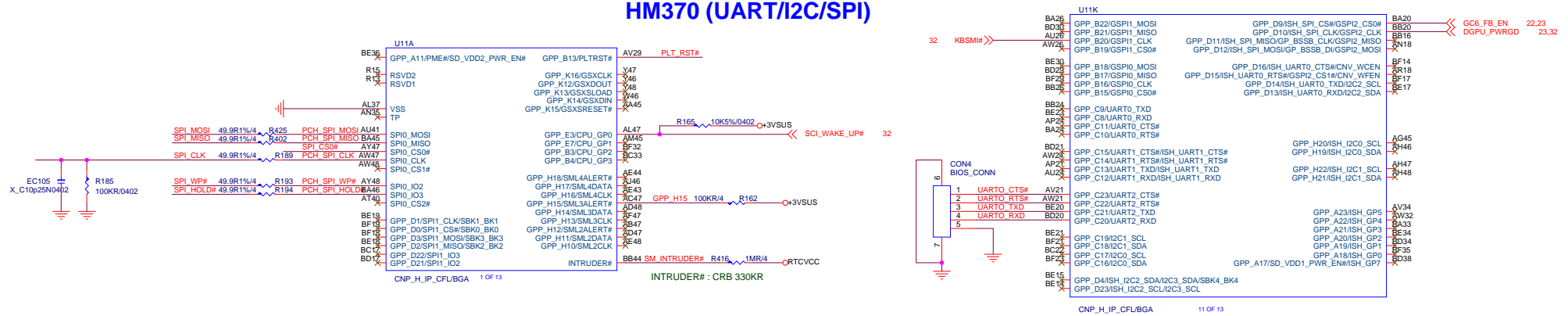
Diagram showing various components and their connections. It includes a table of component assignments for different SKUs (HM370, QM370, CH246) and a table of component assignments for different SKUs (HM370, QM370, CH246).

Component	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
LAN																														
HDD																														
WLAN																														
CardReader																														
M.2 SSD																														
AR(TBT)																														

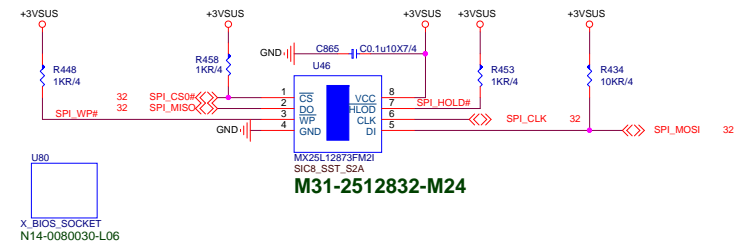
SKU	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030
HM370	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030
QM370	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030
CH246	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030

Title			
PCH-3(HDA/GPIO/TJAG)			
Size	Document Number	Rev	
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HM370 (UART/I2C/SPI)



SPI FLASH ROM



SPI0_IO2

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

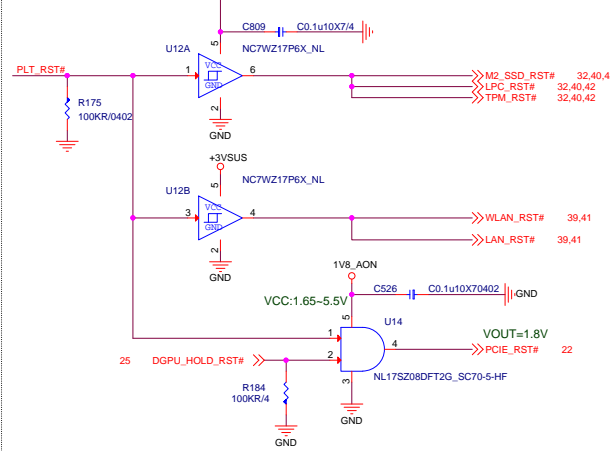
SPI0_IO3

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_MOSI

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

PLT_RST#



GSPI0_MOSI / GPP_B18

The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

GSPI1_MOSI / GPP_B22

This Signal has a weak internal pull-down.	
Bit 6 Boot BIOS	Destination
0	SPI (Default)
1	LPC

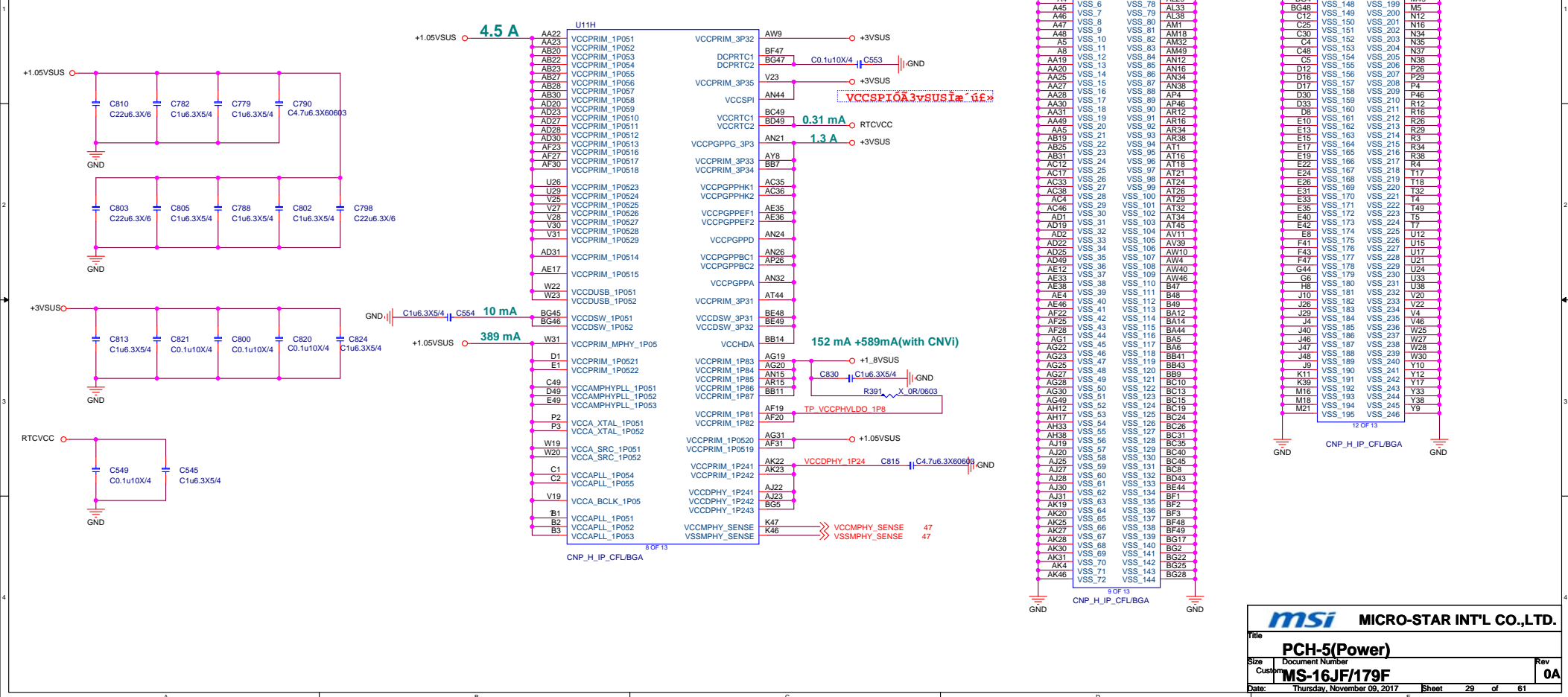
SML2ALERT# / GPP_H12

The signal has a weak internal pull-down. 0 = Master attached Flash sharing enable. (Default) 1 = Slave attached Flash sharing enable	
---	--

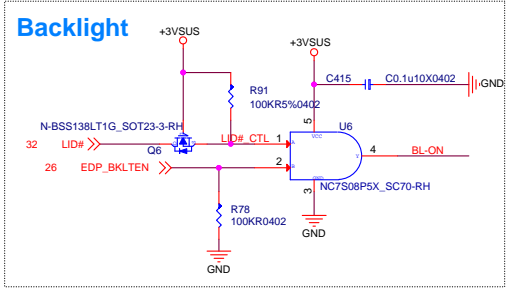
SML3ALERT# / GPP_H15

External pull-up is required.
Recommend 100K if pulled
up to 3.3V or 75K if pulled up to 1.8V.

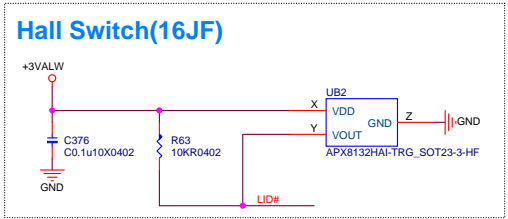
HM370 (Power & GND)



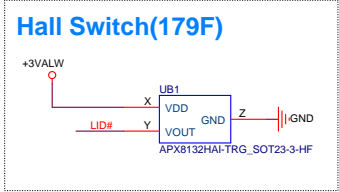
Backlight



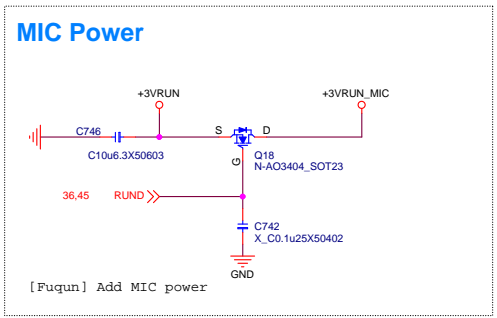
Hall Switch(16JF)



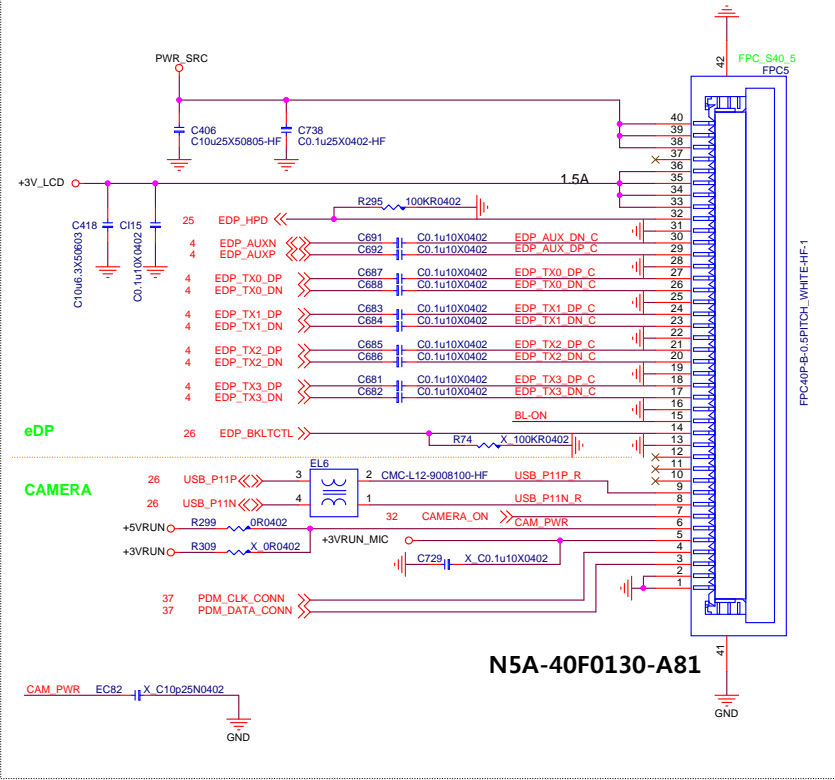
Hall Switch(179F)



MIC Power



eDP CONN
CAMERA



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

MICRO-STAR INT'L CO.,LTD.

Title

eDP /Camera

Size

Document Number

MS-16JF/179F

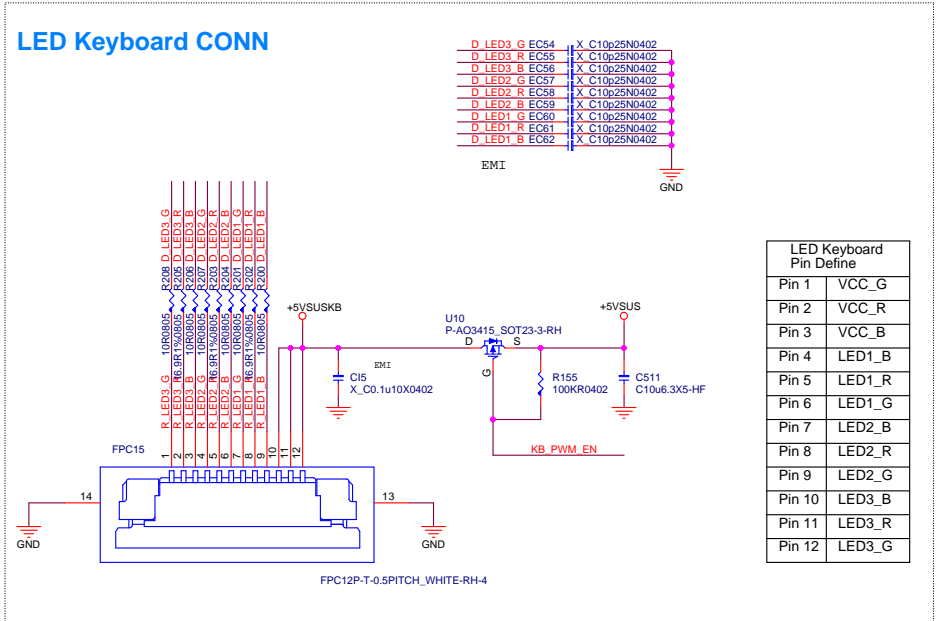
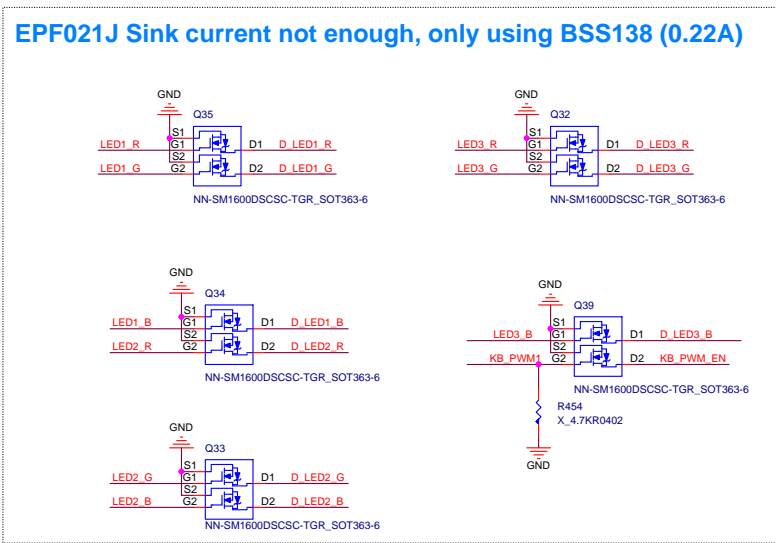
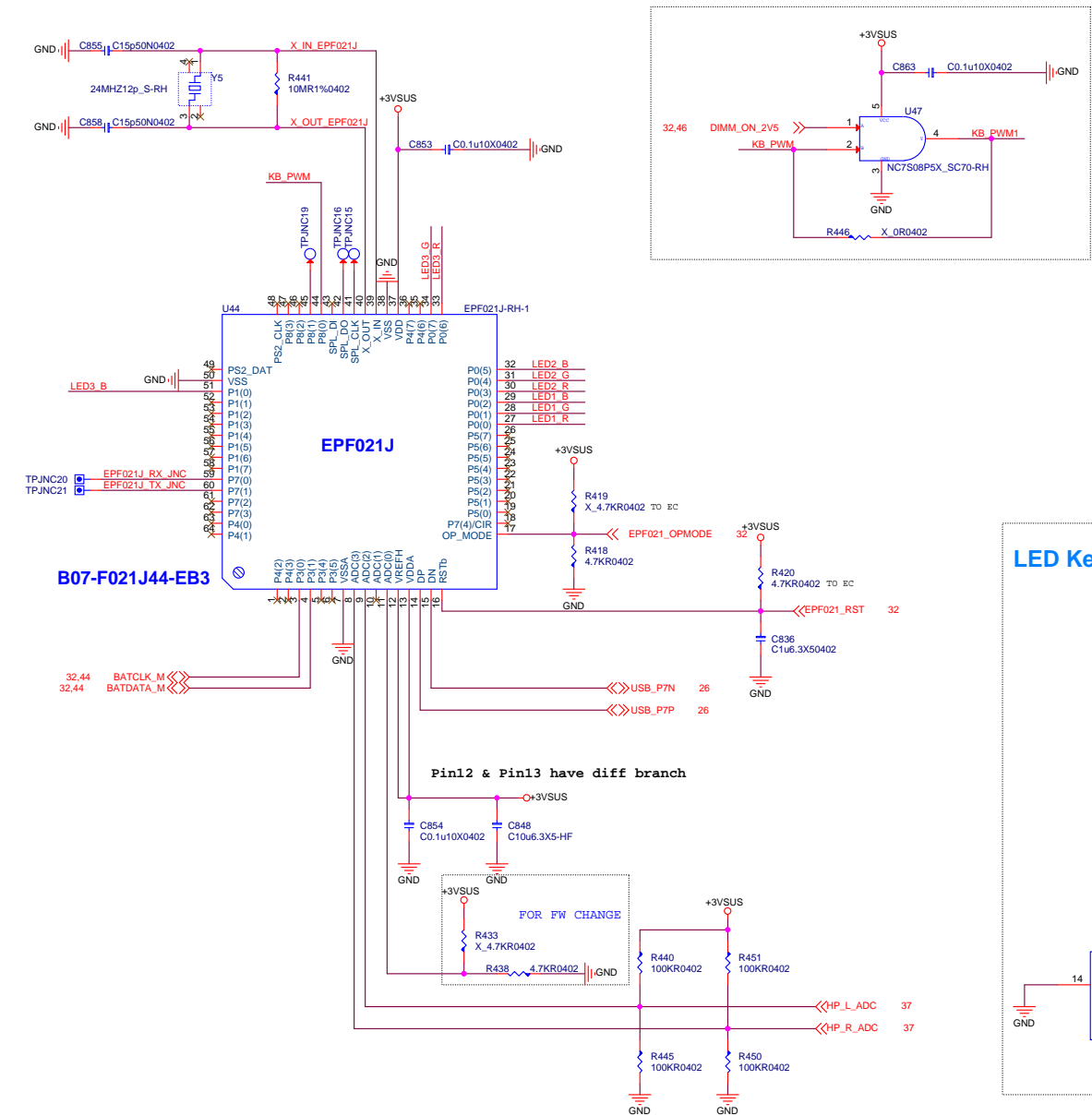
Rev

0A

Date: Thursday, November 09, 2017

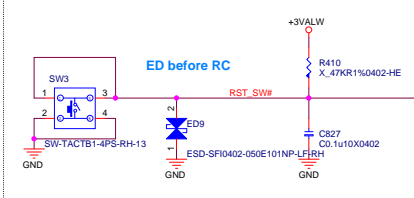
Sheet 30 of 61

LED 8051 Controller

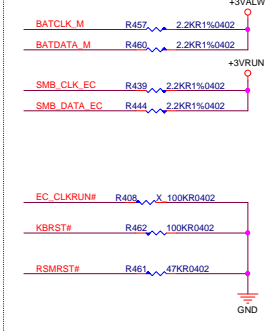


KBC(ENE9028)

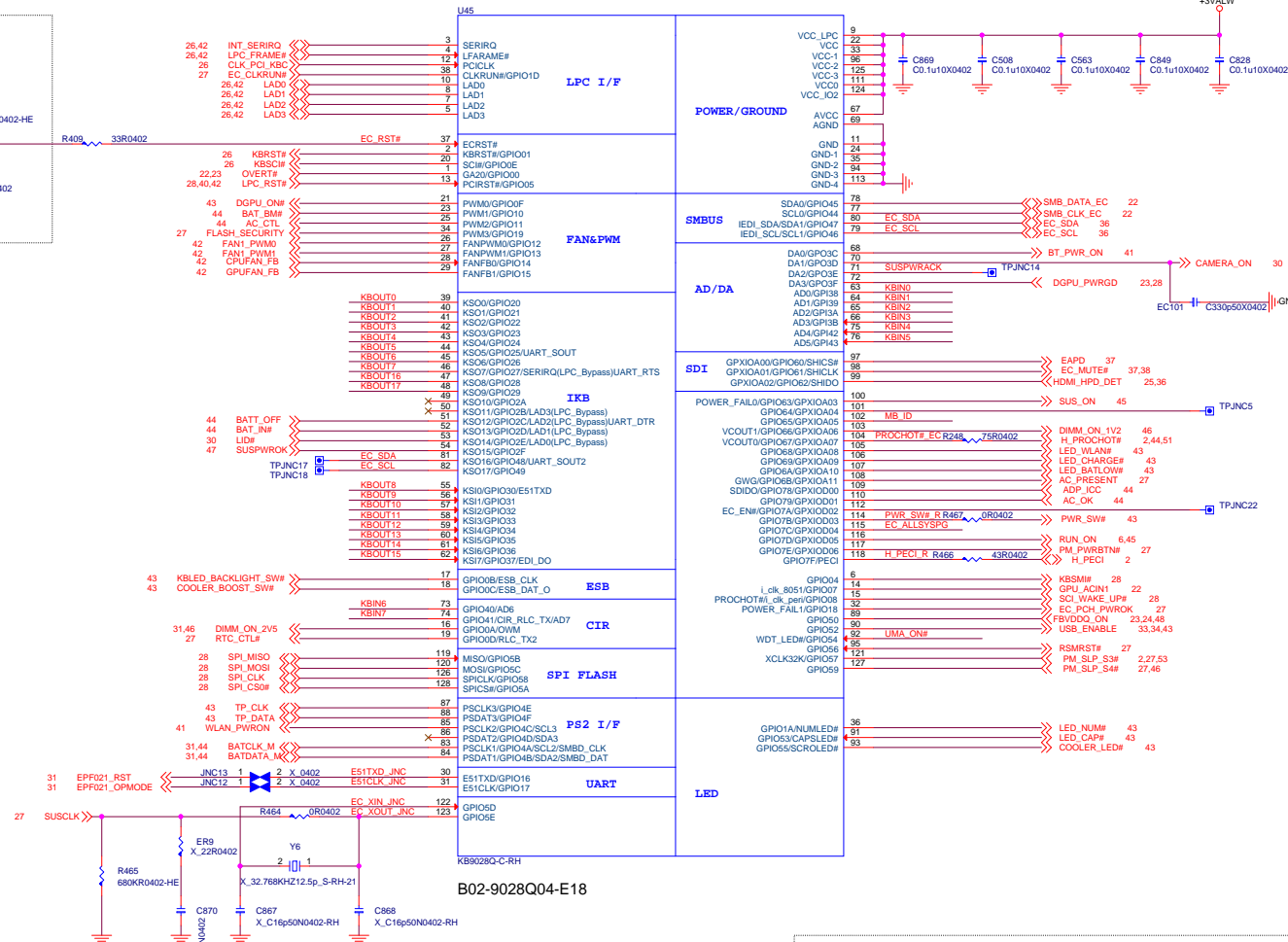
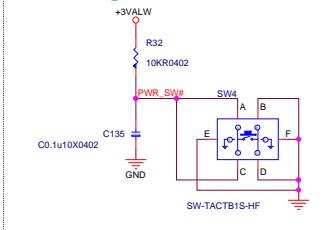
Hardware Reset



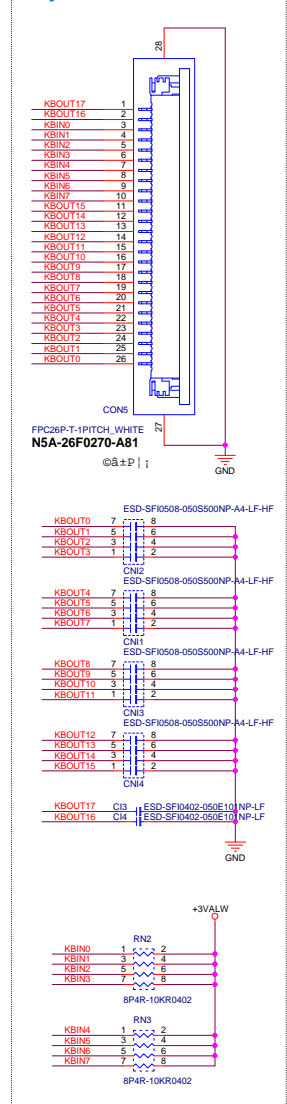
PU/PD



HW Debug



Keyboard conn

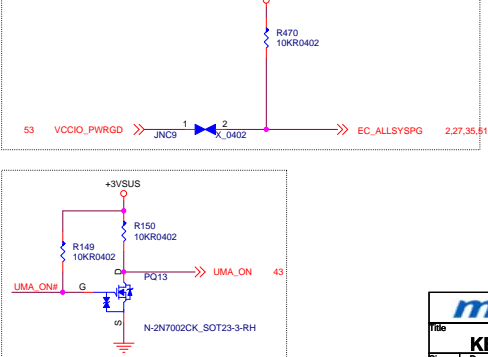


MB_ID	PR293	R463	ID	LAN	HDD
GF62/GF72	NC	10K	0	E2400	MS-16JF: ODD-->16JFA-->HDD MS-179F: HDD
GV62/GV72 62ODM/72ODM	10K	NC	1	AR8171	MS-16JF: ODD-->16JFA-->HDD MS-179F: HDD
PE62/PE72	10K	10K	1/2	AR8171	MS-16JF: ODD-->16JFA-->HDD MS-179F: HDD
	20K	10K	1/3	AR8171	
	10K	20K	2/3		

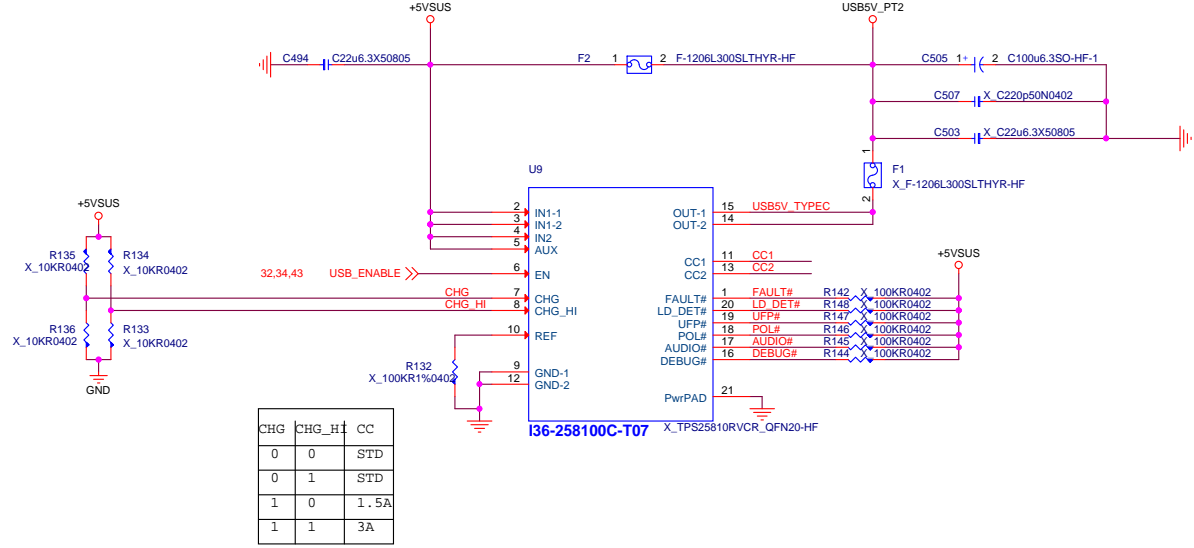
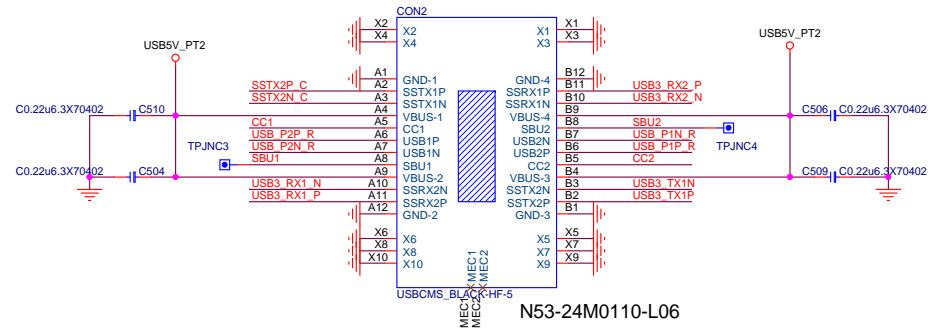
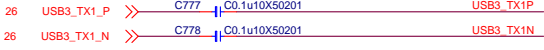
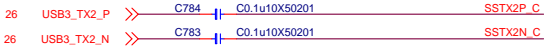
MB_ID



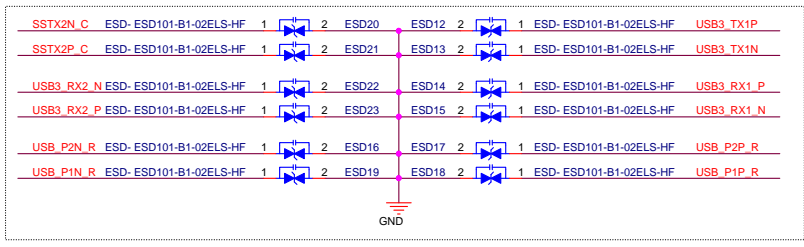
ALLSYSPG



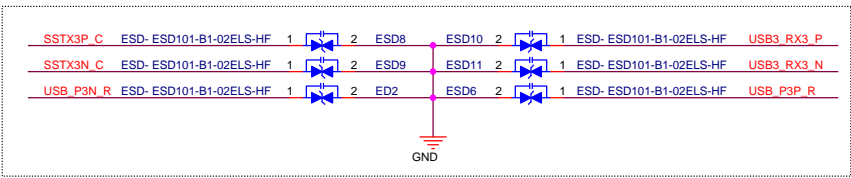
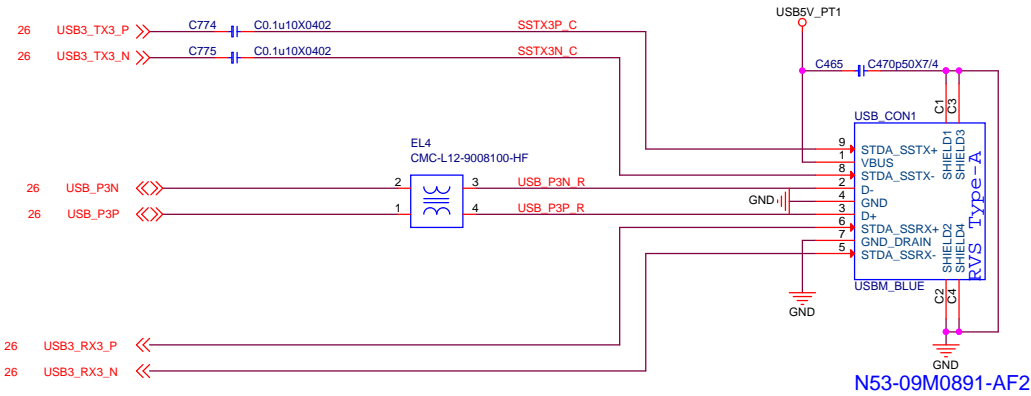
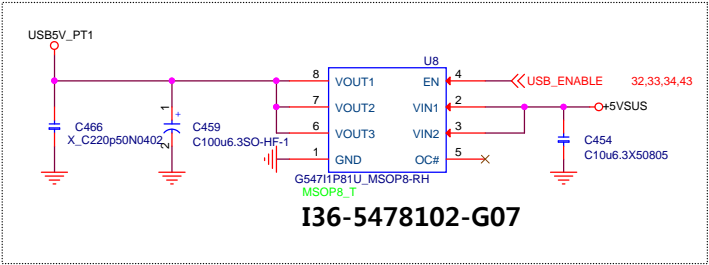
Type-C



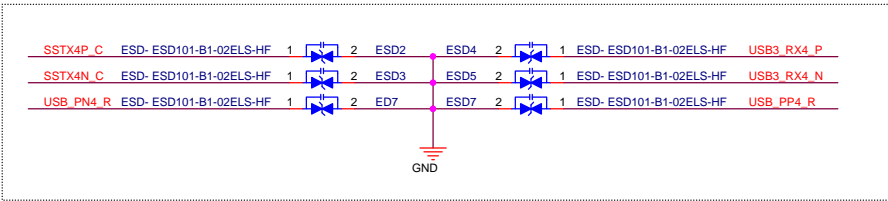
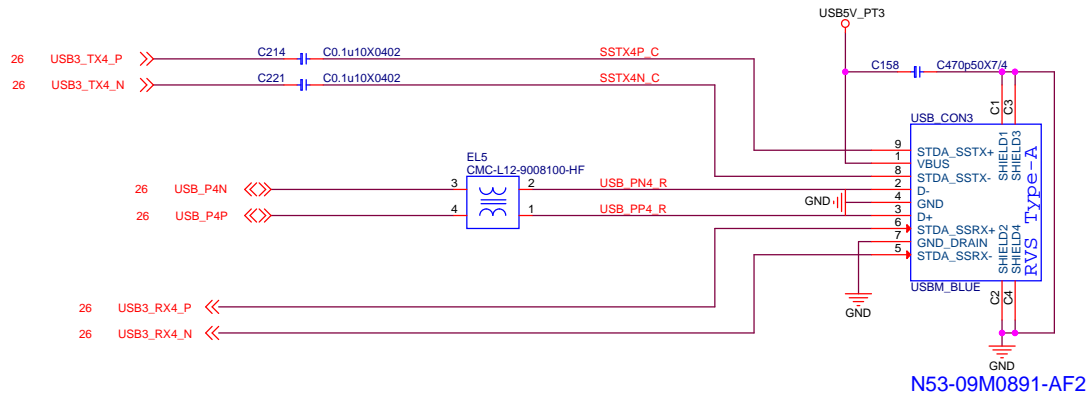
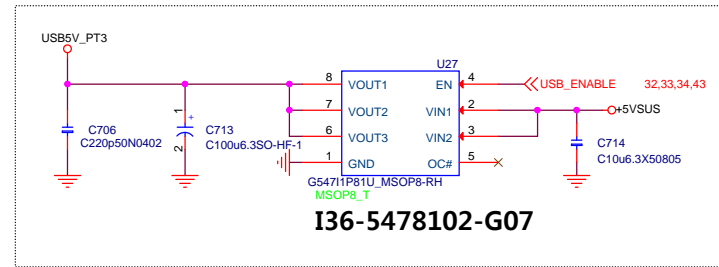
CHG	CHG_HI	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A



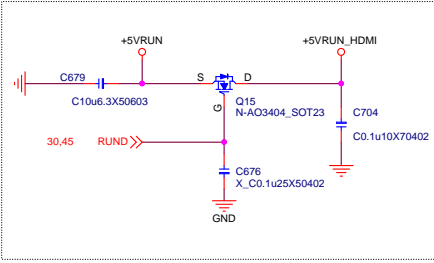
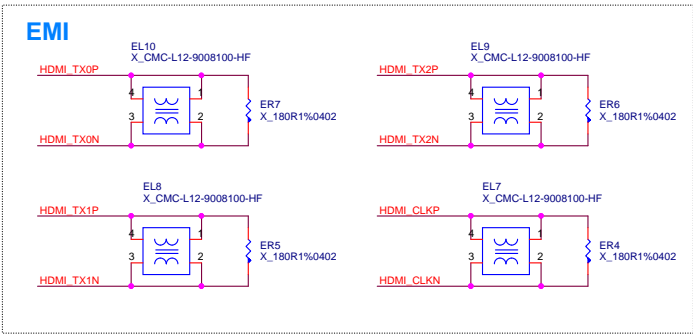
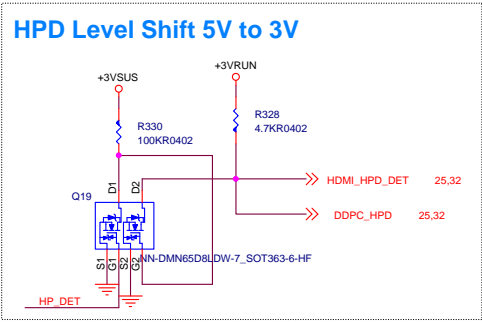
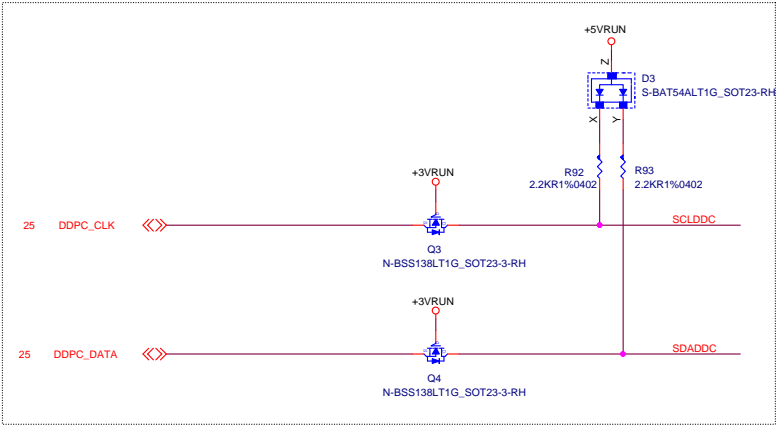
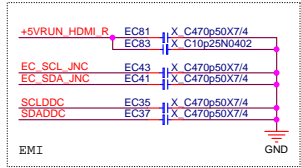
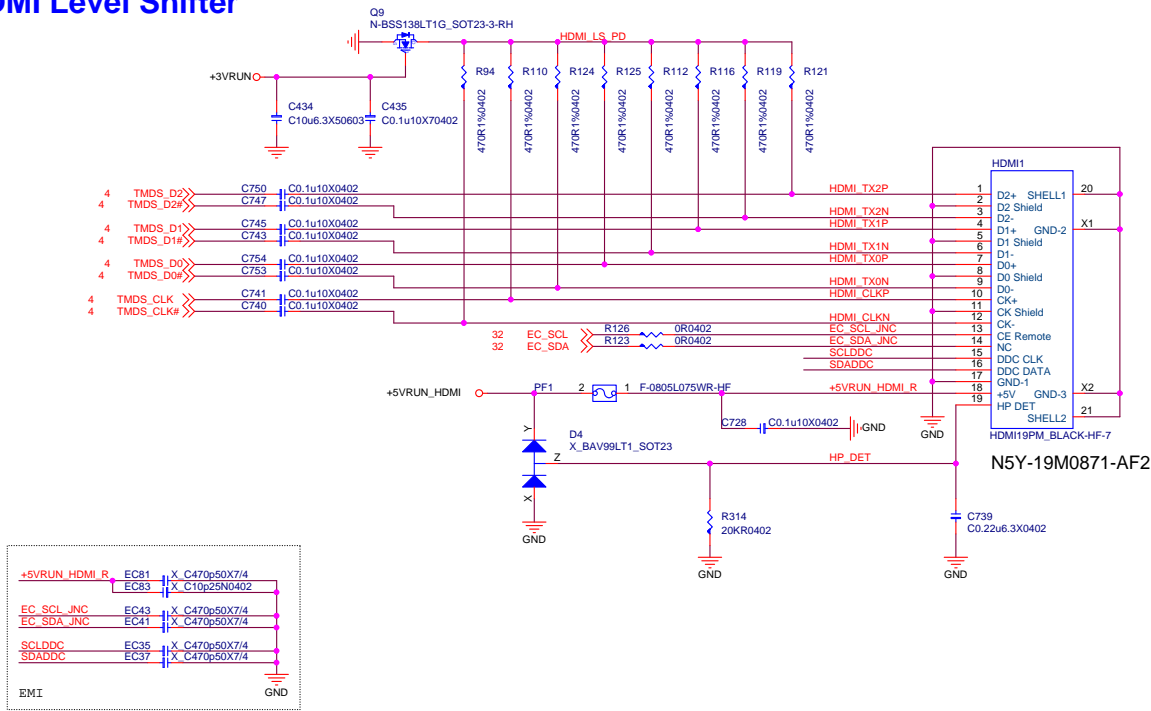
USB3.1 CNT-1



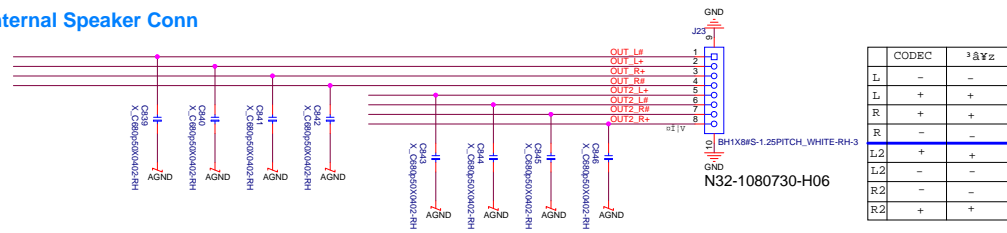
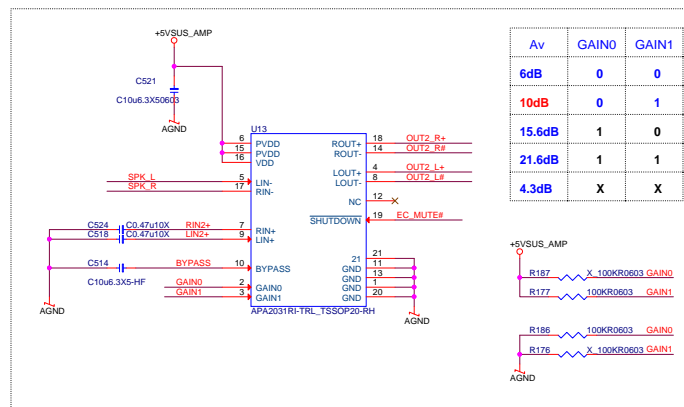
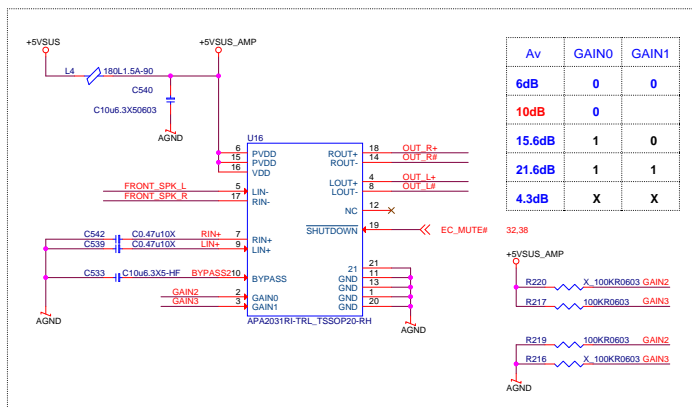
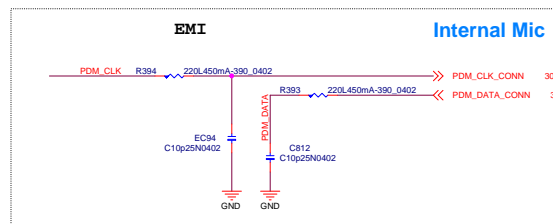
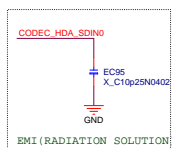
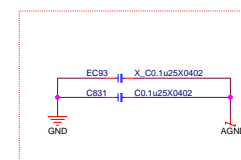
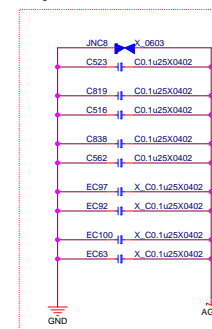
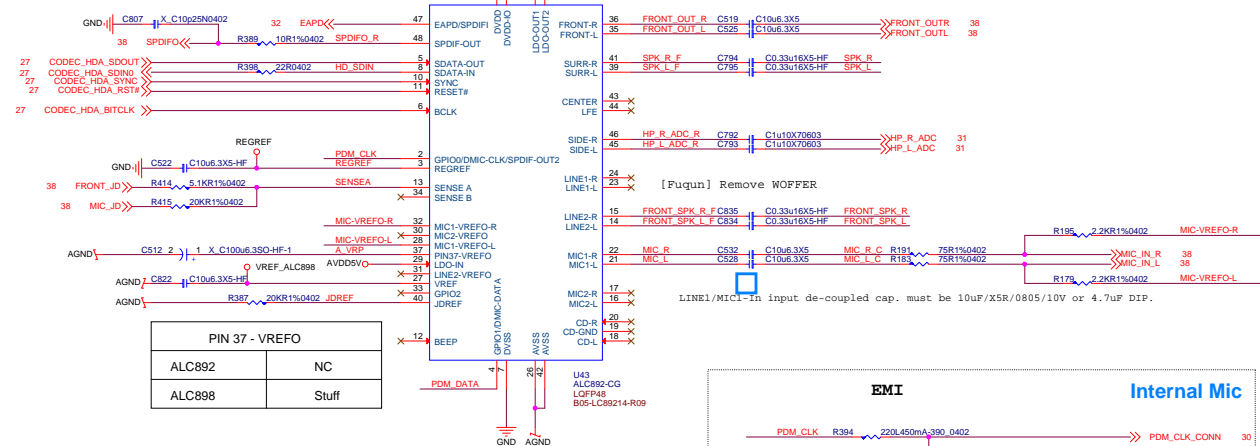
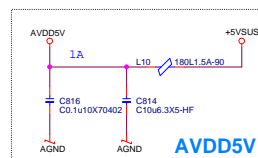
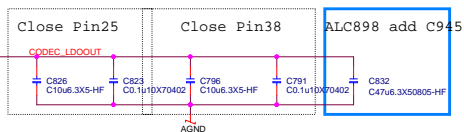
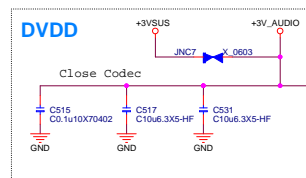
USB3.1 CNT-2



HDMI Level Shifter

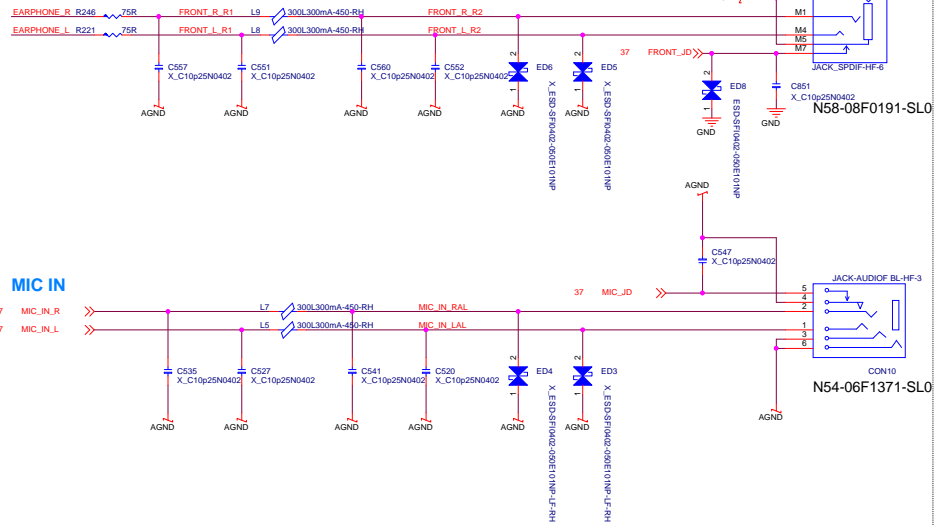


Audio CODEC(ALC892)



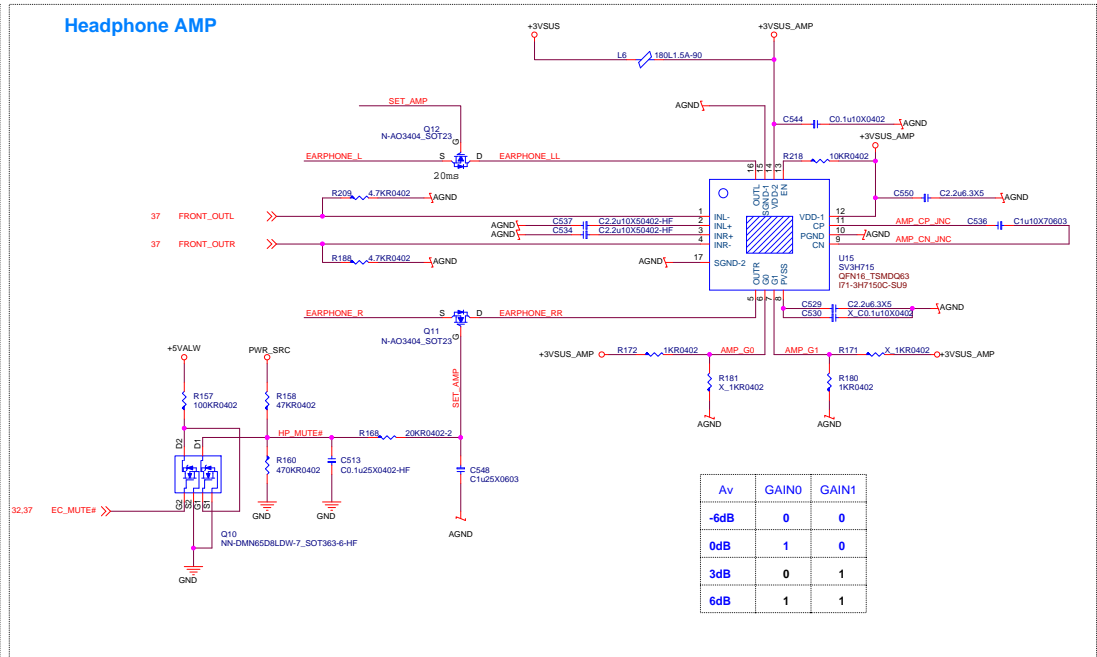
Audio CONN /Woffer

FRONT OUT



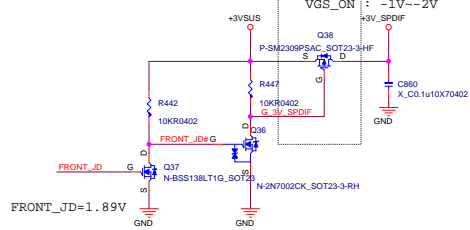
MIC IN

Headphone AMP

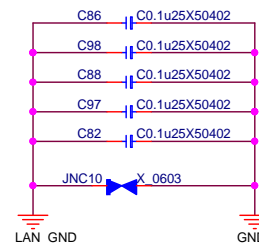
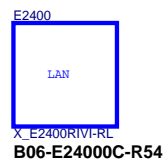
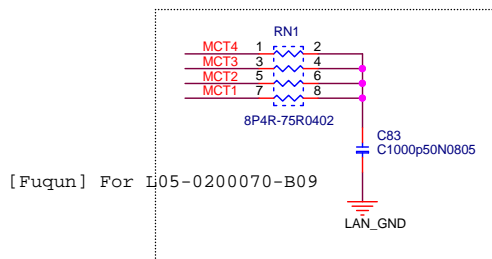
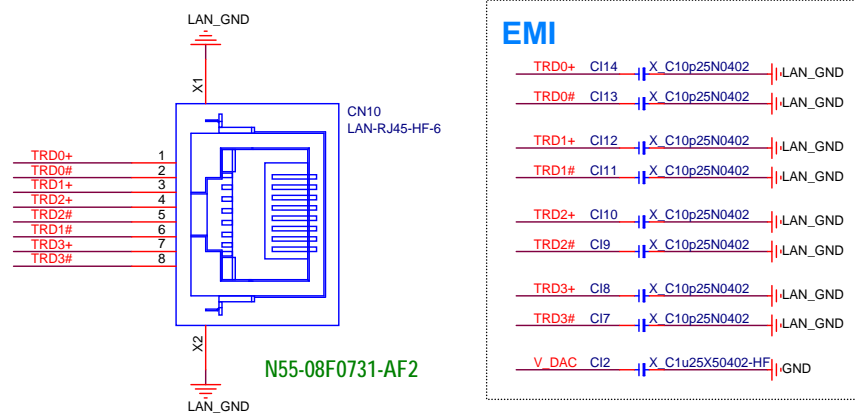
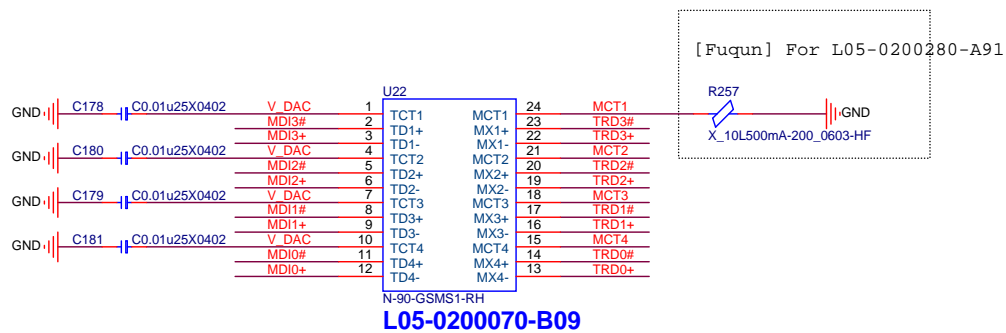
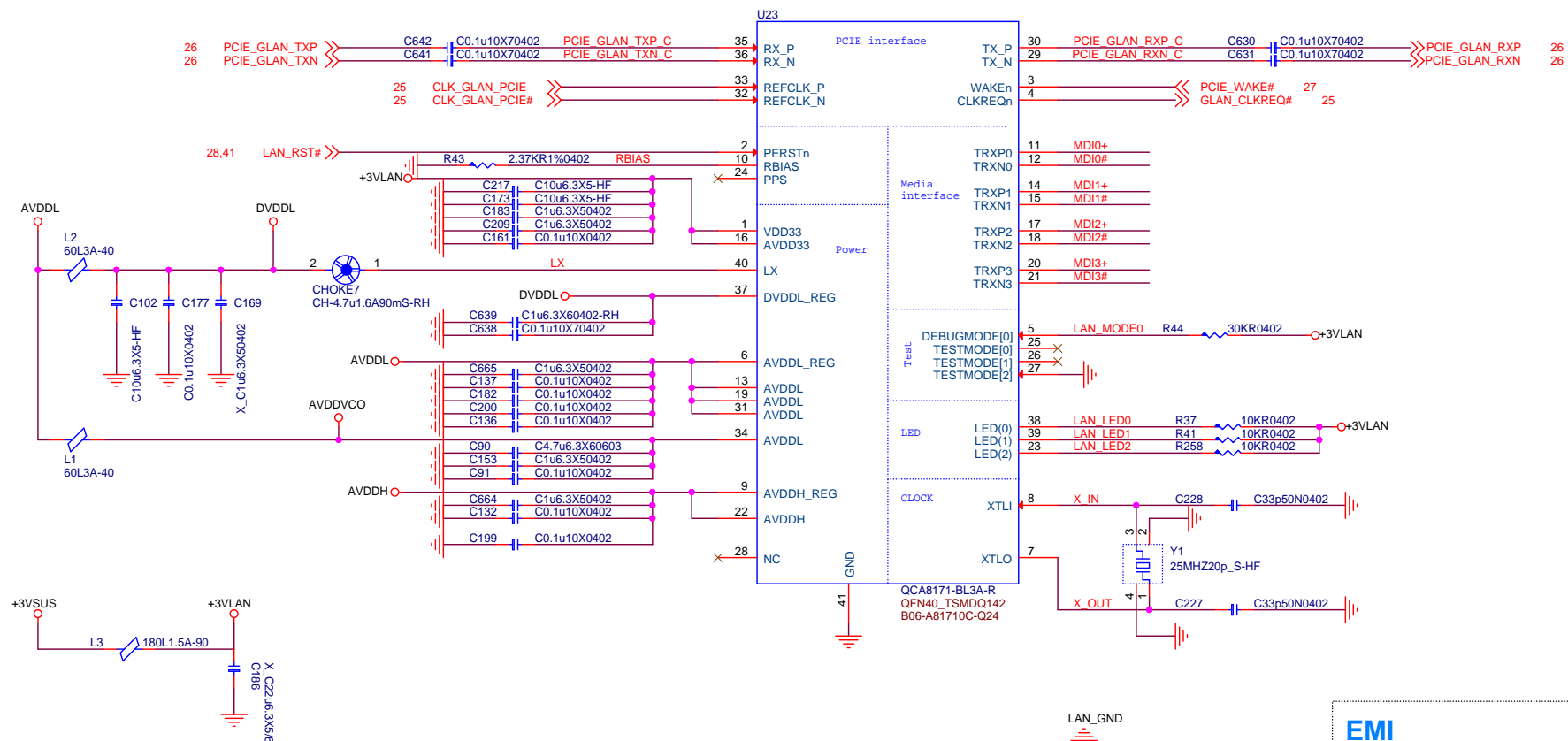


Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

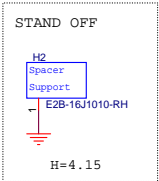
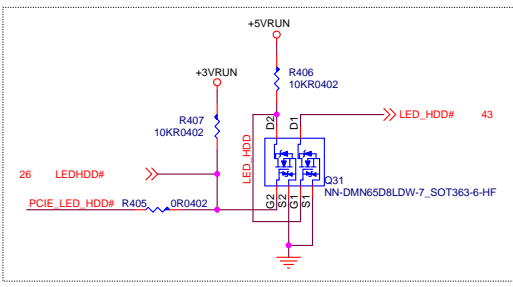
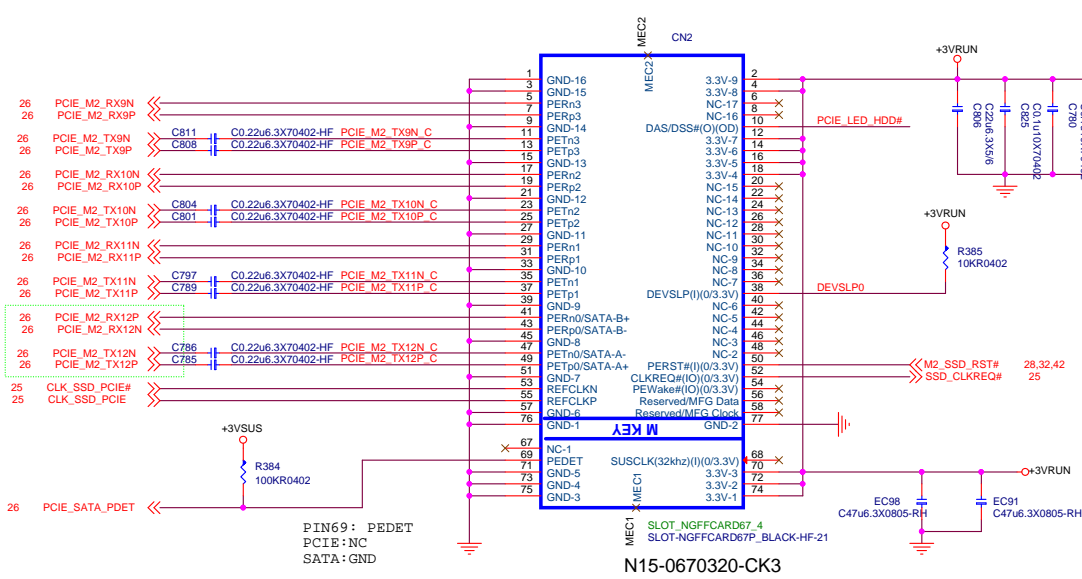
SPDIF Power



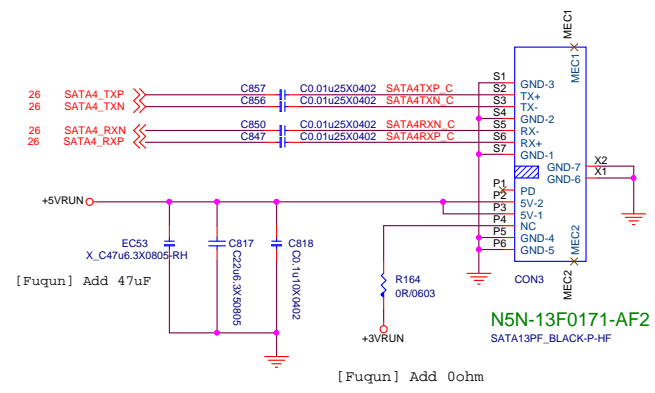
LAN(AR8171/E2400)



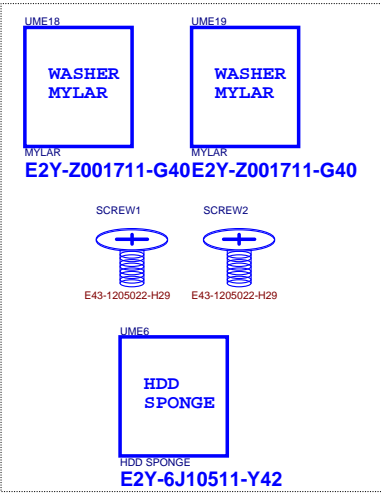
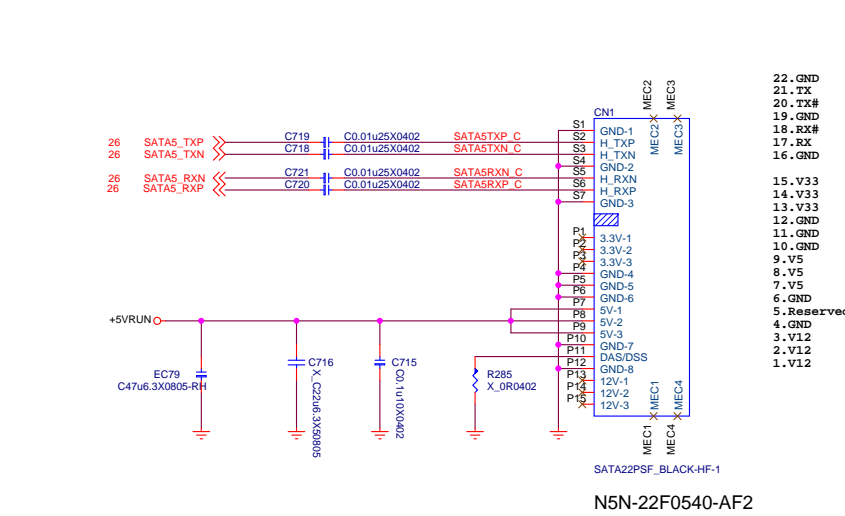
SSD



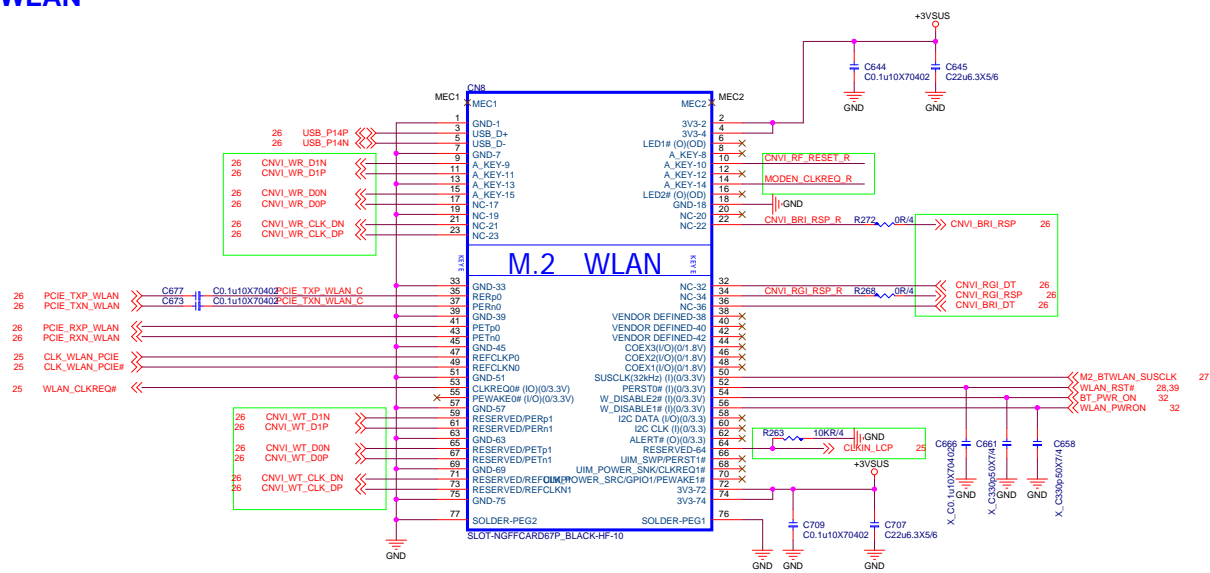
HDD(MS-16JF)



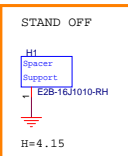
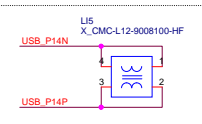
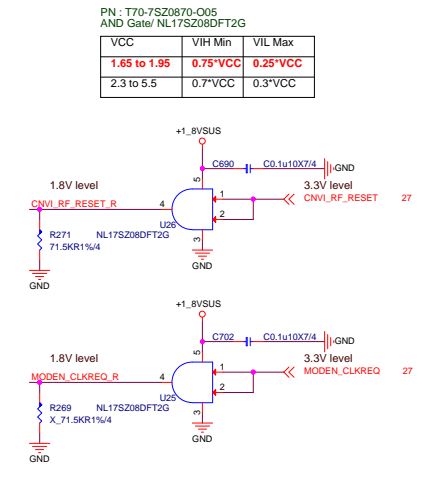
HDD(MS-179F)



WLAN

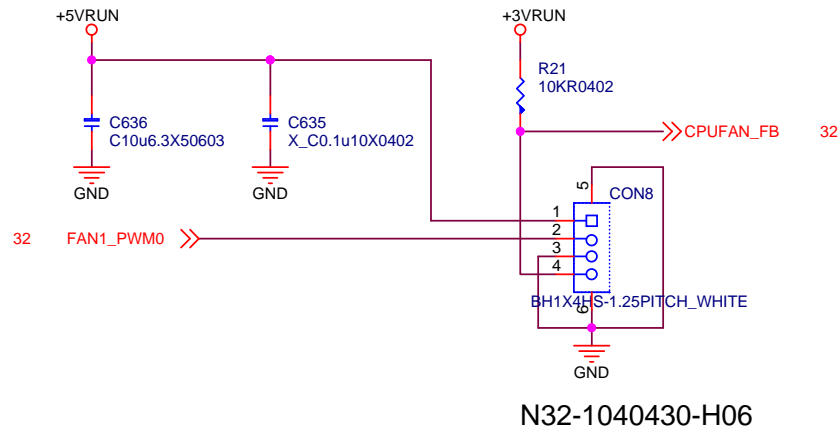


(Level Shifter 3.3V to 1.8V)

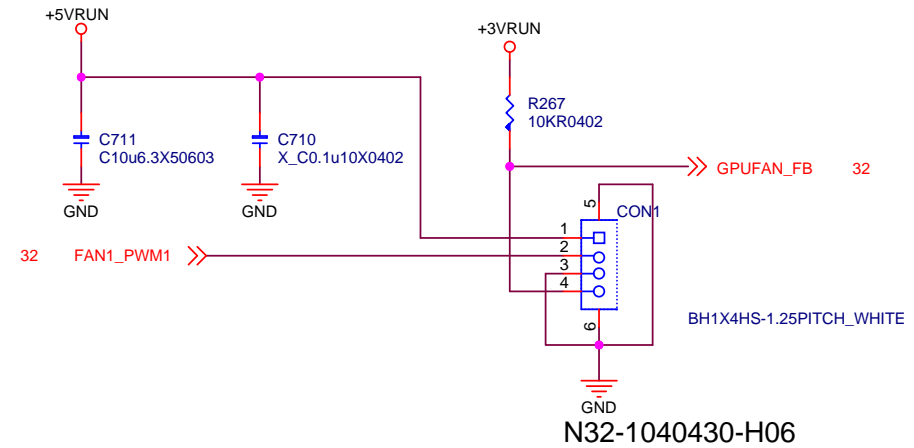


Pin #	M.2 WLAN	INTEL CNV1 WLAN	Pin #	M.2 WLAN	INTEL CNV1 WLAN
Pin 1	GND	GND	Pin 2	3.3V	3.3V
Pin 3	USB_D+	N/C	Pin 4	3.3V	3.3V
Pin 5	USB_D-	N/C	Pin 6	LED1#	LED1#
Pin 7	GND	GND	Pin 8	Module Key	N/C
Pin 9	Module Key	WGR_D1N	Pin 10	Module Key	RF_RESET_B(1.8V)
Pin 11	Module Key	WGR_D1P	Pin 12	Module Key	N/C
Pin 13	Module Key	GND	Pin 14	Module Key	CLKREQ0(1.8V)
Pin 15	Module Key	WGR_D0N	Pin 16	LED2#	LED2#
Pin 17	N/C	WGR_D0P	Pin 18	GND	GND
Pin 19	N/C	GND	Pin 20	N/C	N/C
Pin 21	N/C	WGR_CLKN	Pin 22	N/C	BRI_RSP(1.8V)
Pin 23	N/C	WGR_CLKP	Pin 24	Module Key	Module Key
Pin 25	Module Key	Module Key	Pin 26	Module Key	Module Key
Pin 27	Module Key	Module Key	Pin 28	Module Key	Module Key
Pin 29	Module Key	Module Key	Pin 30	Module Key	Module Key
Pin 31	Module Key	Module Key	Pin 32	N/C	RGI_DT(1.8V)
Pin 33	GND	GND	Pin 34	N/C	RGI_RSP(1.8V)
Pin 35	PERP0	N/C	Pin 36	N/C	BGI_DT(1.8V)
Pin 37	PERN0	N/C	Pin 38	N/C	N/C
Pin 39	GND	GND	Pin 40	N/C	N/C
Pin 41	PETP0	N/C	Pin 42	N/C	N/C
Pin 43	PETN0	N/C	Pin 44	N/C	N/C
Pin 45	GND	GND	Pin 46	N/C	N/C
Pin 47	REFCLKP0	N/C	Pin 48	N/C	N/C
Pin 49	REFCLKN0	N/C	Pin 50	SUSCLK (32KHz)	SUSCLK (32KHz)
Pin 51	GND	GND	Pin 52	PERST0#	N/C
Pin 53	CLKREQ0#	N/C	Pin 54	BT_EN (W_DISABLE2#)	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	N/C	Pin 56	WLAN_EN (W_DISABLE2#)	WLAN_EN (W_DISABLE2#)
Pin 57	GND	GND	Pin 58	N/C	N/C
Pin 59	N/C	WT_D1N	Pin 60	N/C	N/C
Pin 61	N/C	WT_D1P	Pin 62	N/C	N/C
Pin 63	GND	GND	Pin 64	Resever	REFCLK0(38.4MKz)
Pin 65	N/C	WT_D0N	Pin 66	N/C	N/C
Pin 67	N/C	WT_D0P	Pin 68	N/C	N/C
Pin 69	GND	GND	Pin 70	N/C	N/C
Pin 71	N/C	WT_CLKN	Pin 72	3.3V	3.3V
Pin 73	N/C	WT_CLKP	Pin 74	3.3V	3.3V
Pin 75	GND	GND			

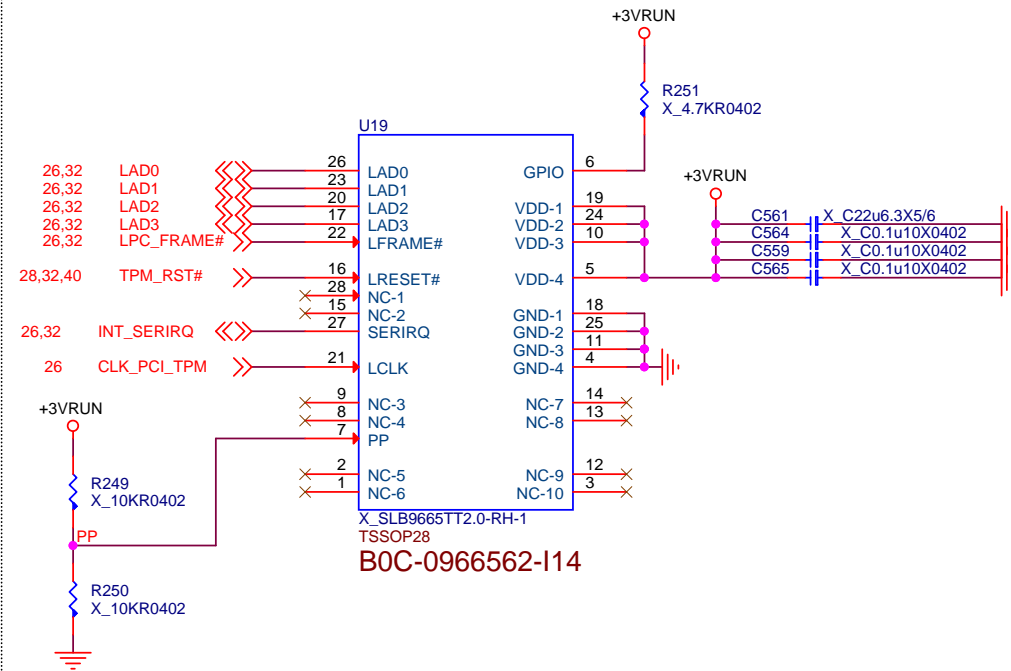
CPU FAN



GPU FAN



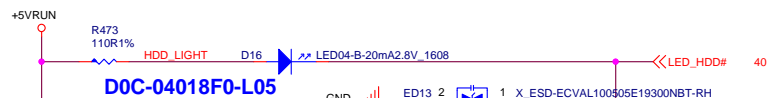
TPM



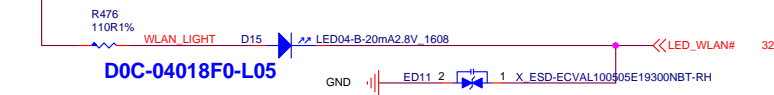
Title		
ODD/HDD/FAN		
Size	Document Number	Rev
Custom	MS-16JE/179F	0A
Date:	Monday, November 27, 2017	Sheet 42 of 61

LED for 16JF

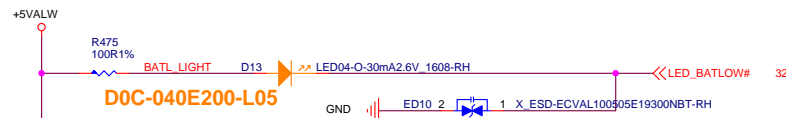
Blue
(HDD)



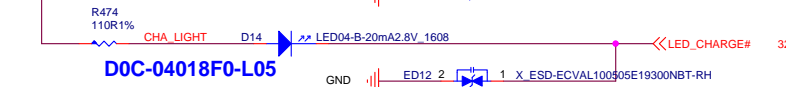
Blue
(WLAN)



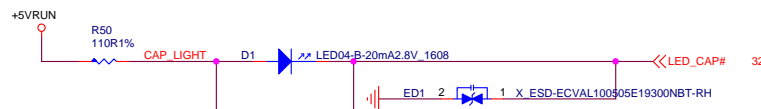
ORANGE
(BATLOW)



Blue
(CHARGE)



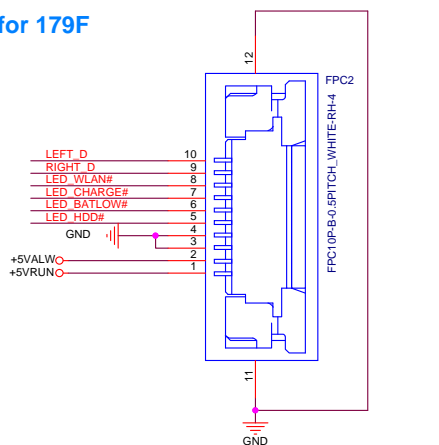
Blue
(CAP)



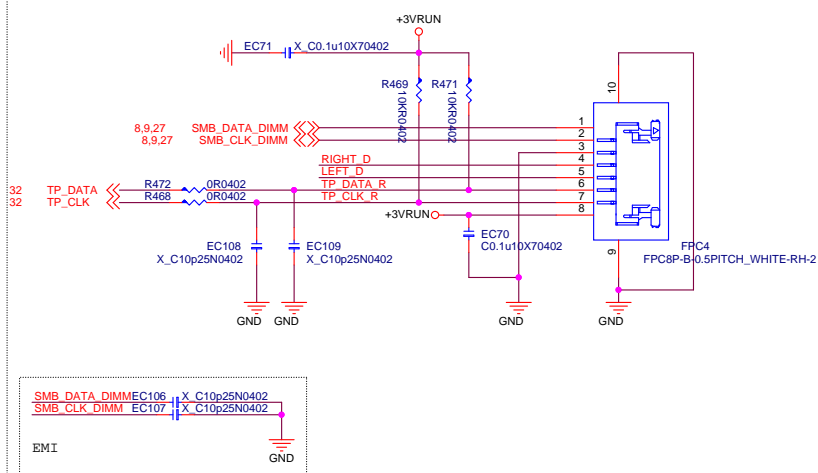
LED for 179F (16Mx remove)

D0C-04018F0-L05

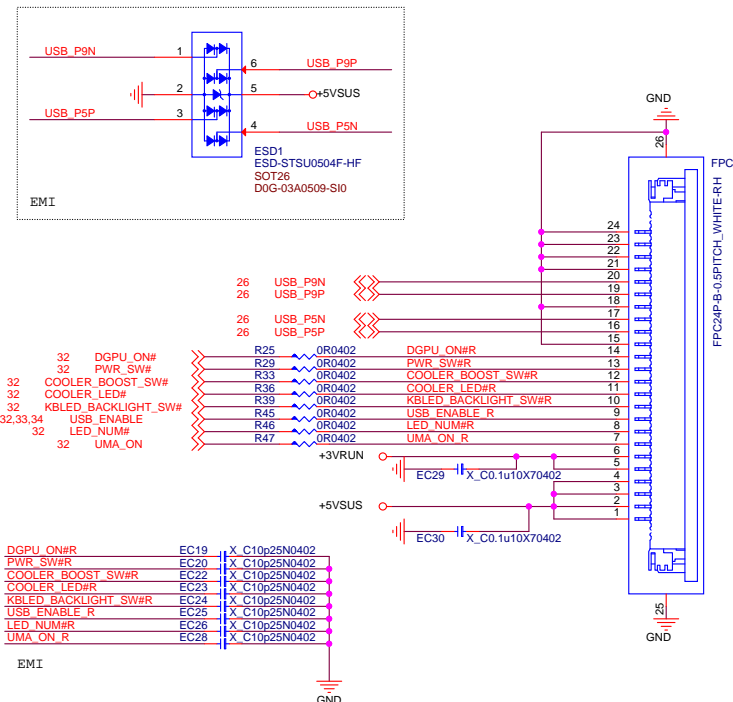
LED for 179F



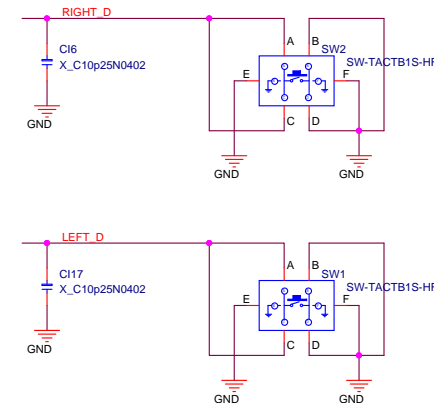
Touch Pad



16JF2/179F2

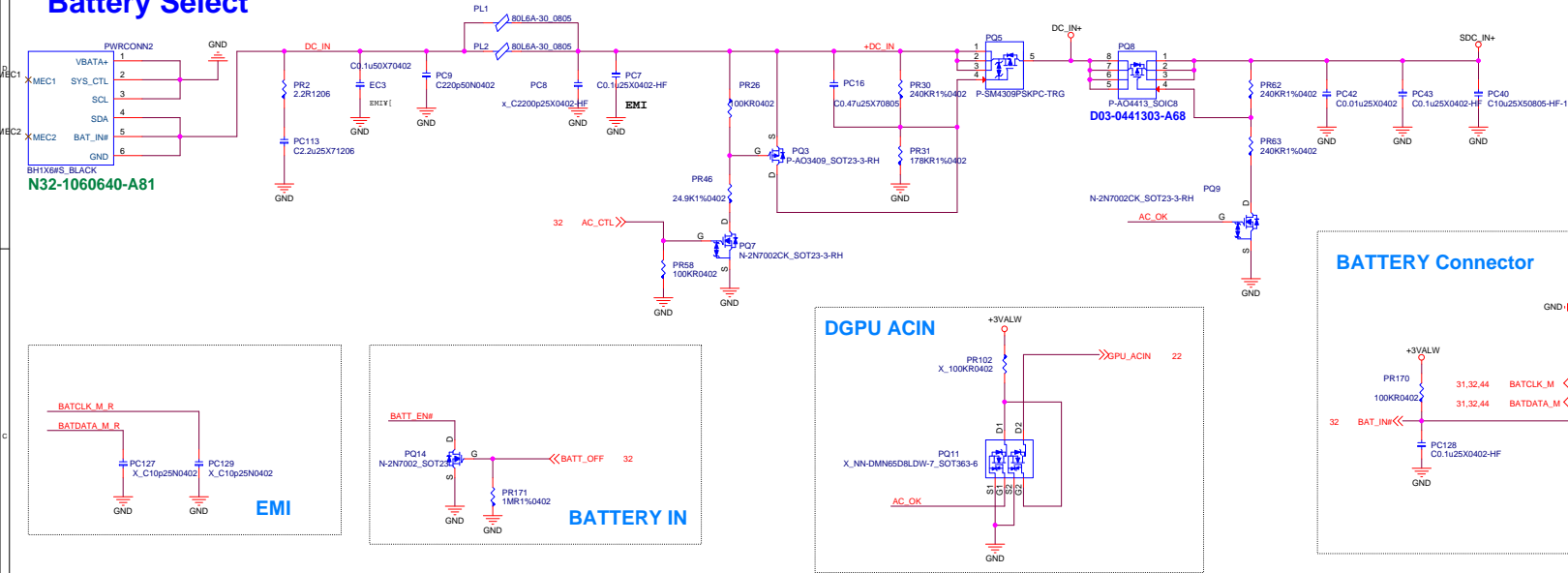


16JF



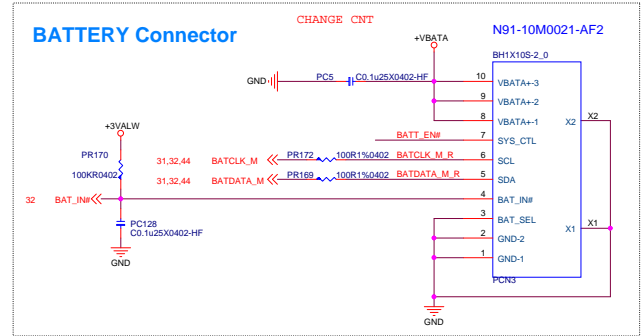
Battery Select/Charger

Battery Select

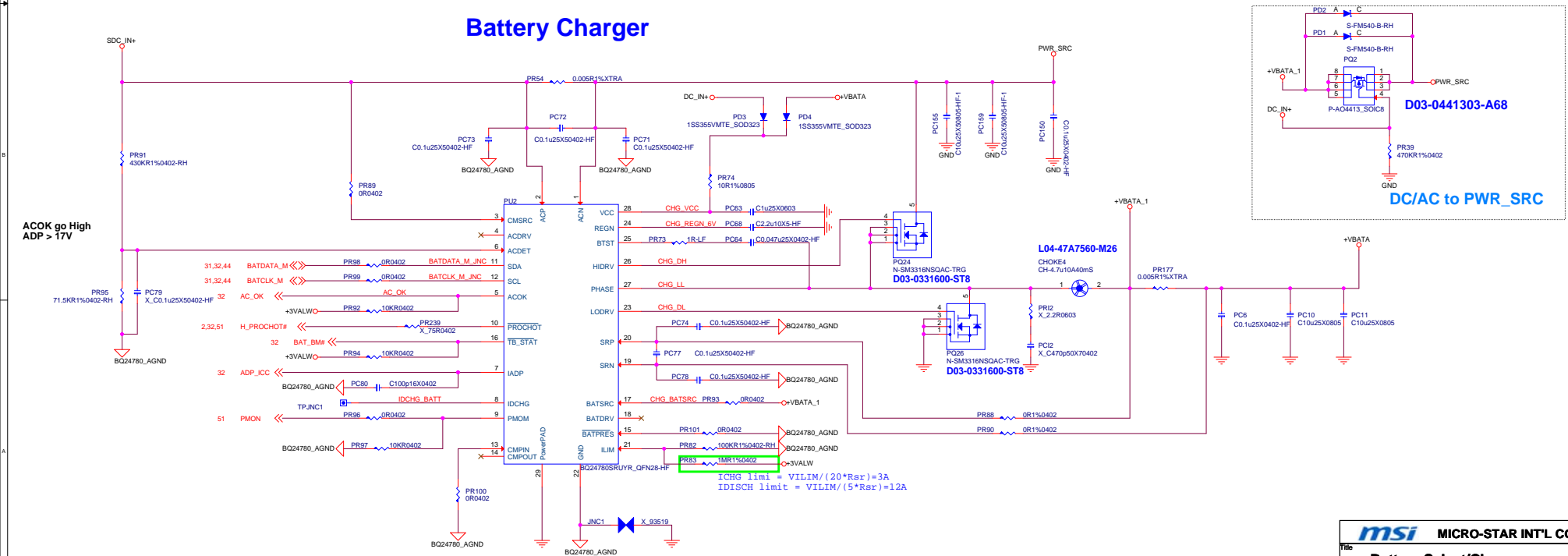


BATTERY Connector

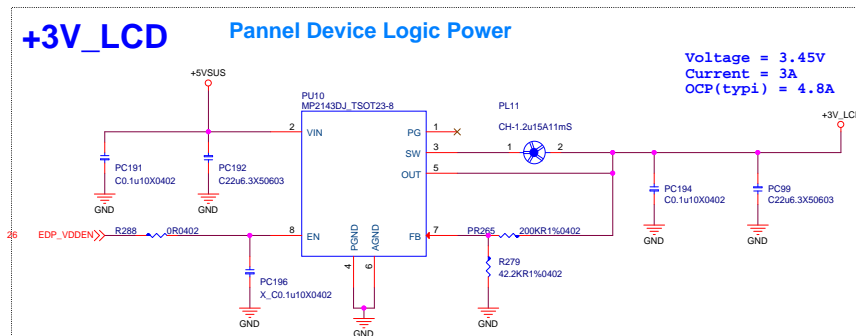
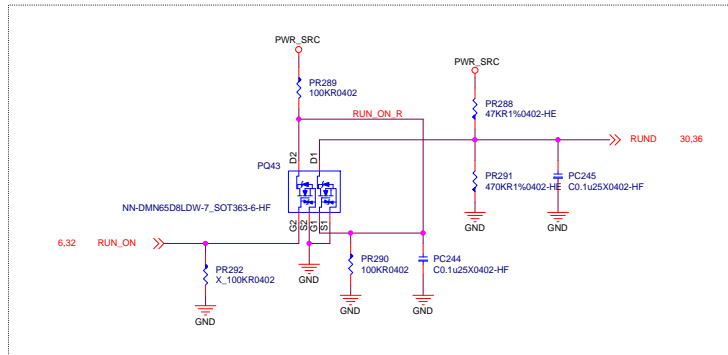
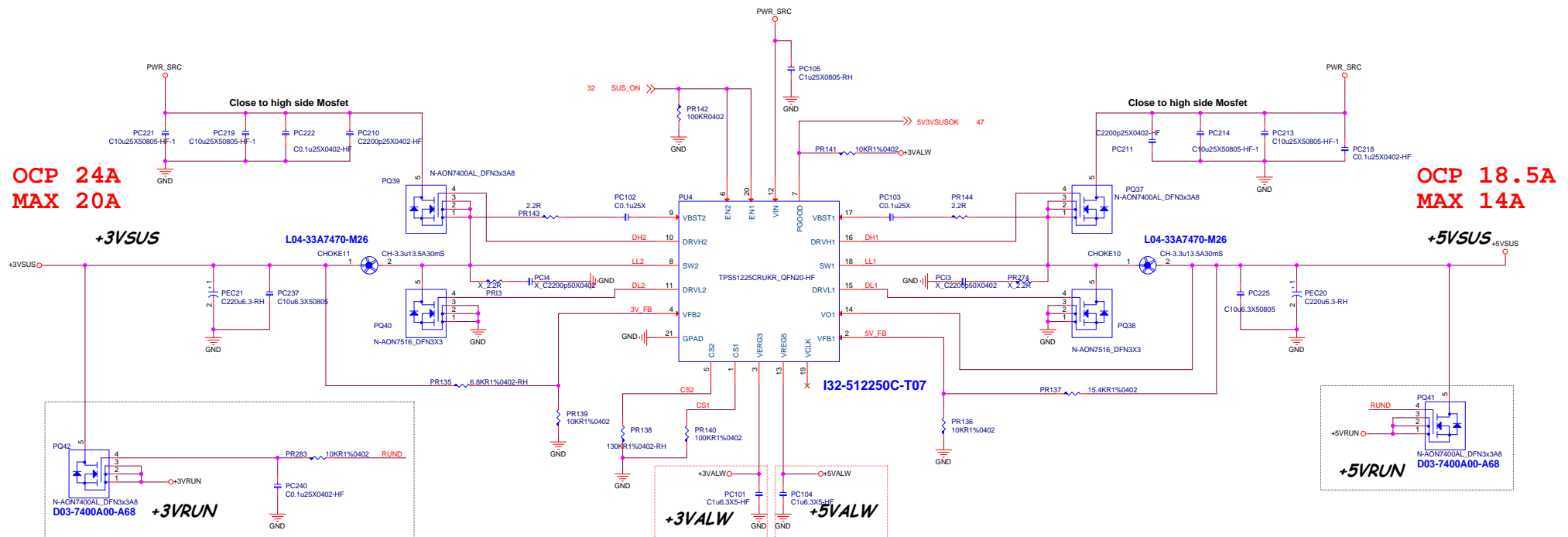
CHANGE CNT



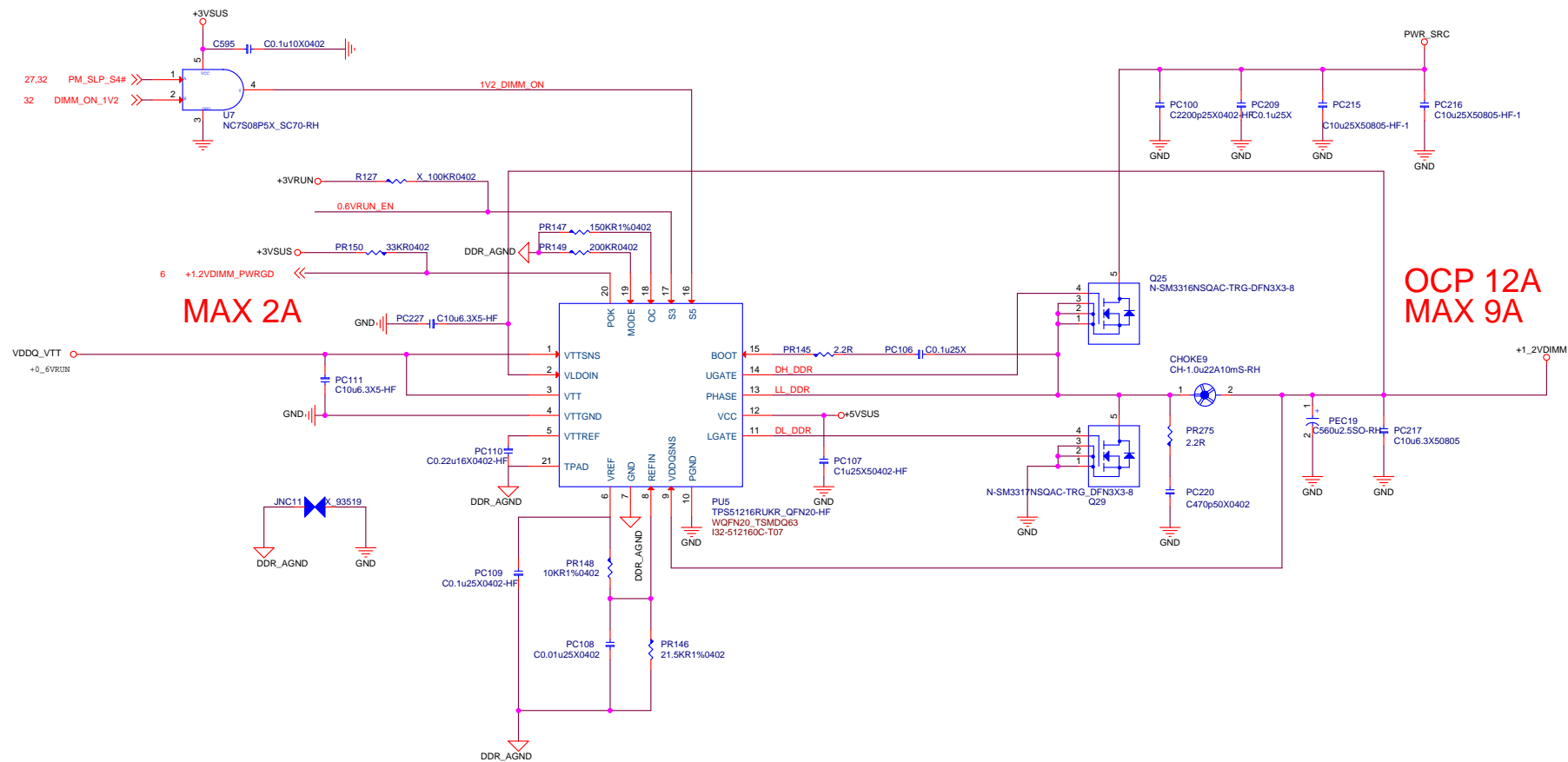
Battery Charger



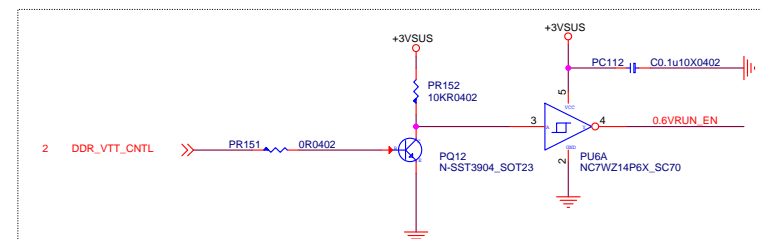
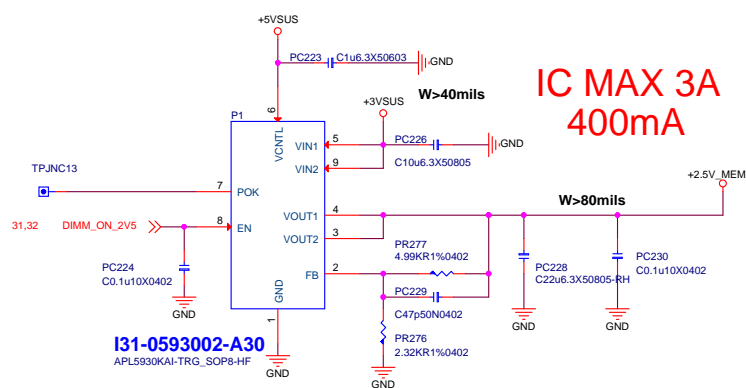
System Power



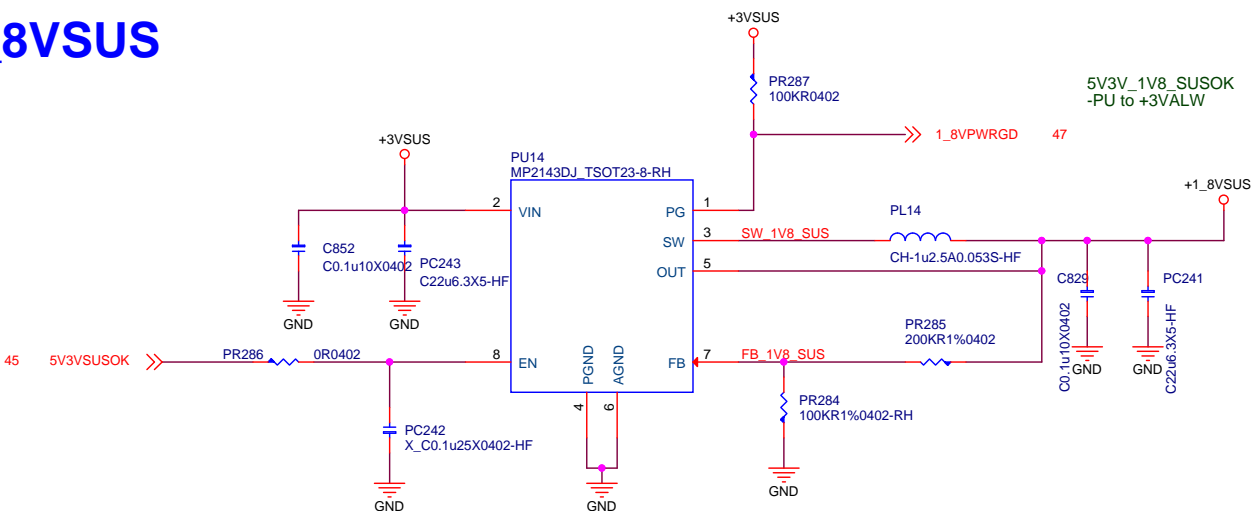
+1_2VDIMM/+0.6VRUN




+2.5V_MEM

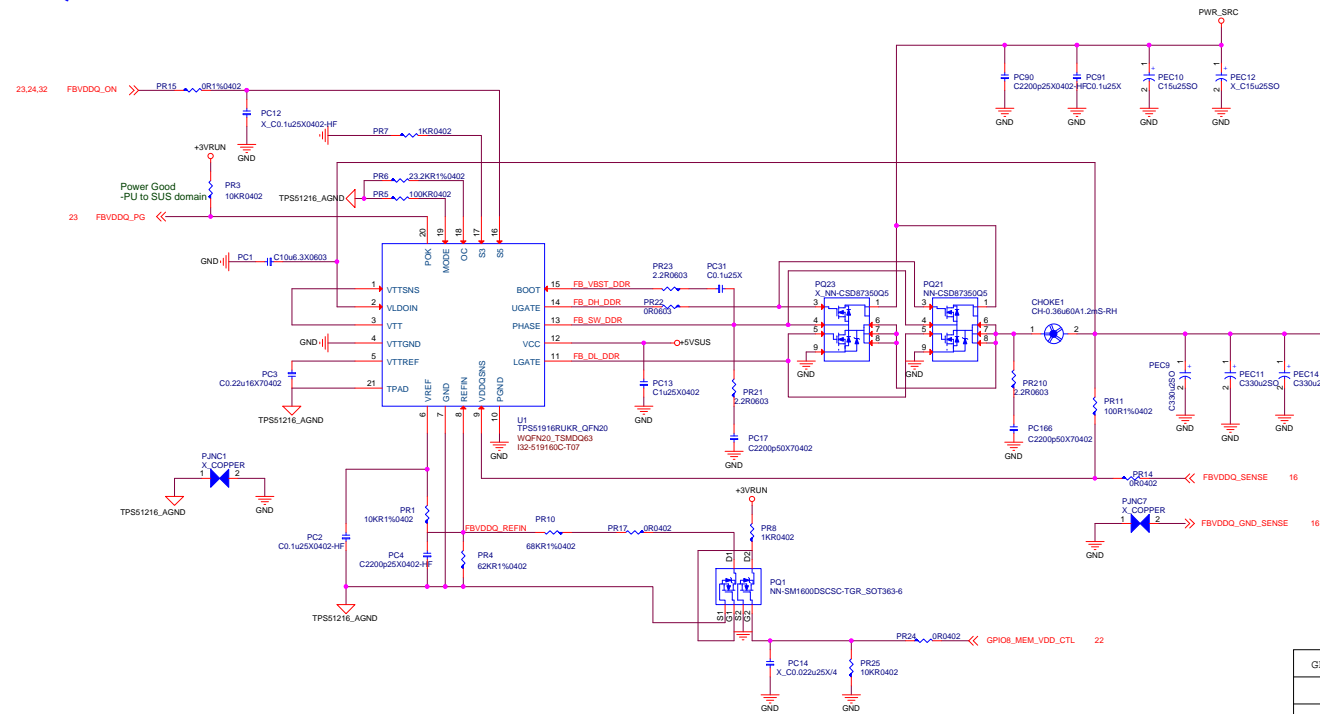


+1_8VSUS



 MICRO-STAR INT'L CO.,LTD.	
Title	
1.05VSUS /PEX VDD/1.8VSUS	
Size	Document Number MS-16JF/179F
Date:	Thursday, November 09, 2017 Sheet 47 of 61 Rev 0A

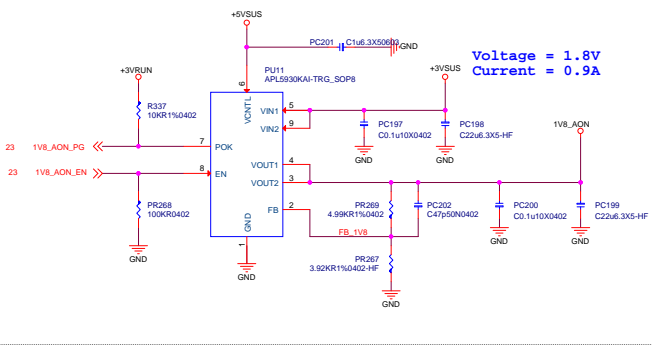
FBVDDQ



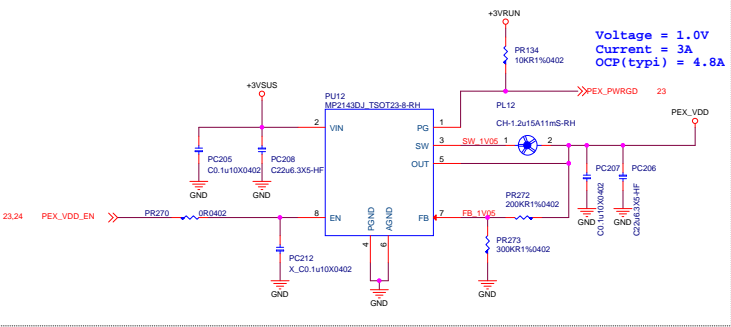
OCF 25A
MAX 11A

EDP-Peak 20A
EDP-Con 11A

1V8_AON



PEX_VDD



DGPU POWER / UP9509P

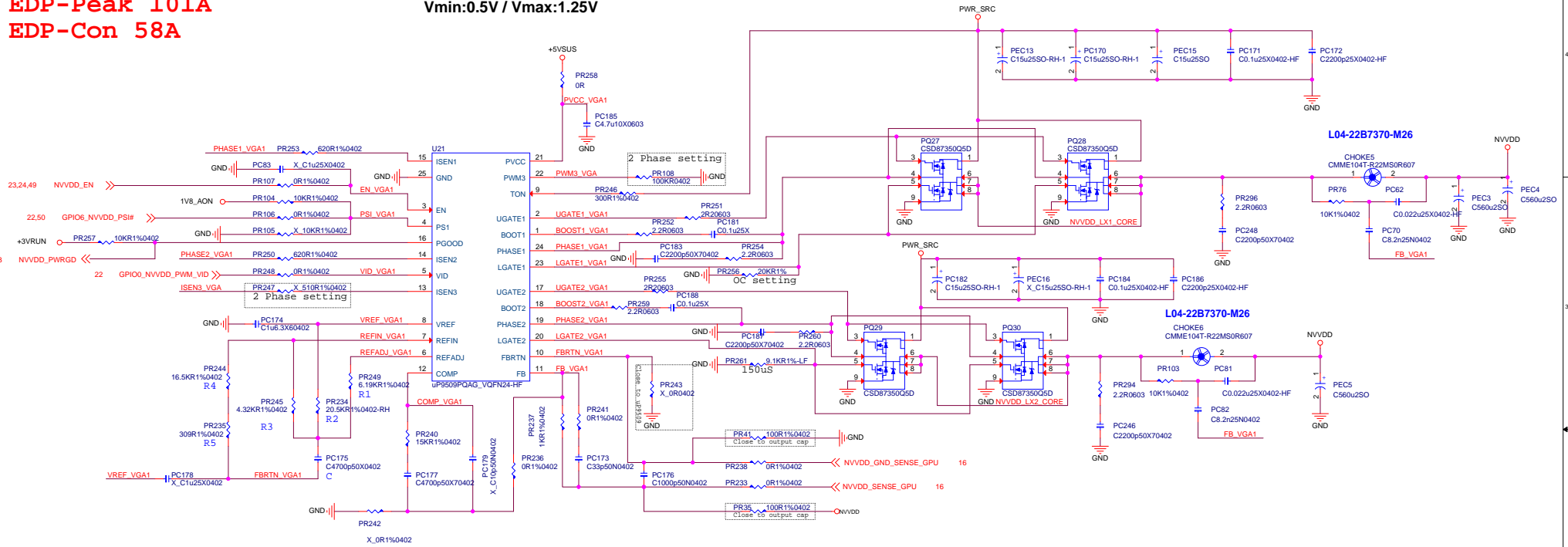
EDP-Peak 101A

EDP-Con 58A

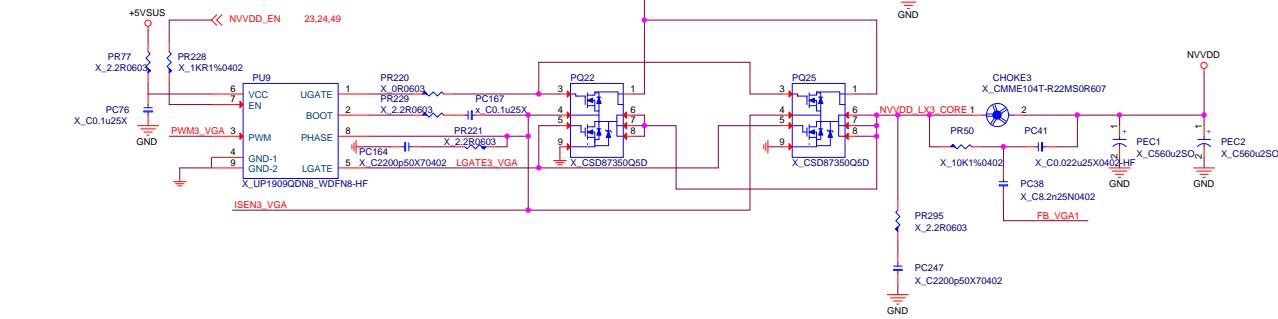
DGPU POWER NVVDD

VBoot:0.8V

Vmin:0.5V / Vmax:1.25V

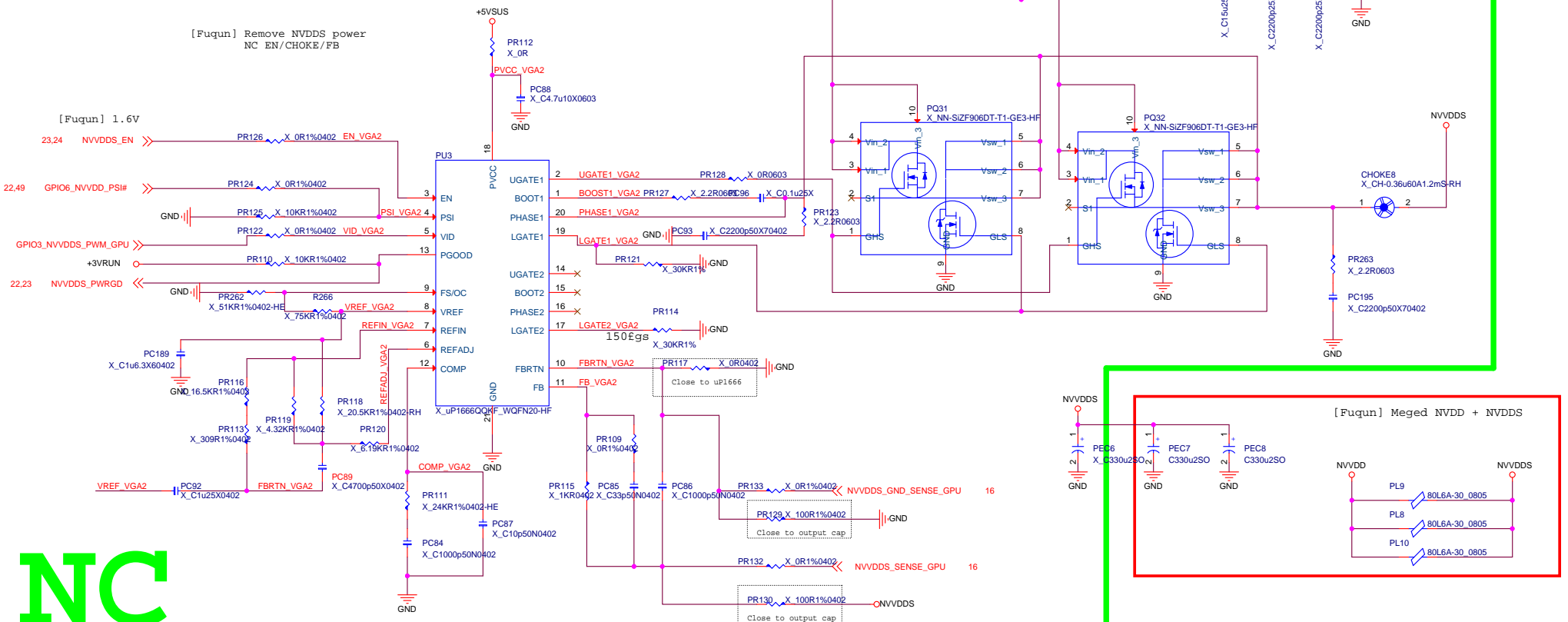


CONFIG	R1	R2	R3	R4	R5	C
N17P-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF




EDP-Peak 18A
EDP-Con 13A

VBoot:0.8V
Vmin:0.5V / Vmax:1.25V

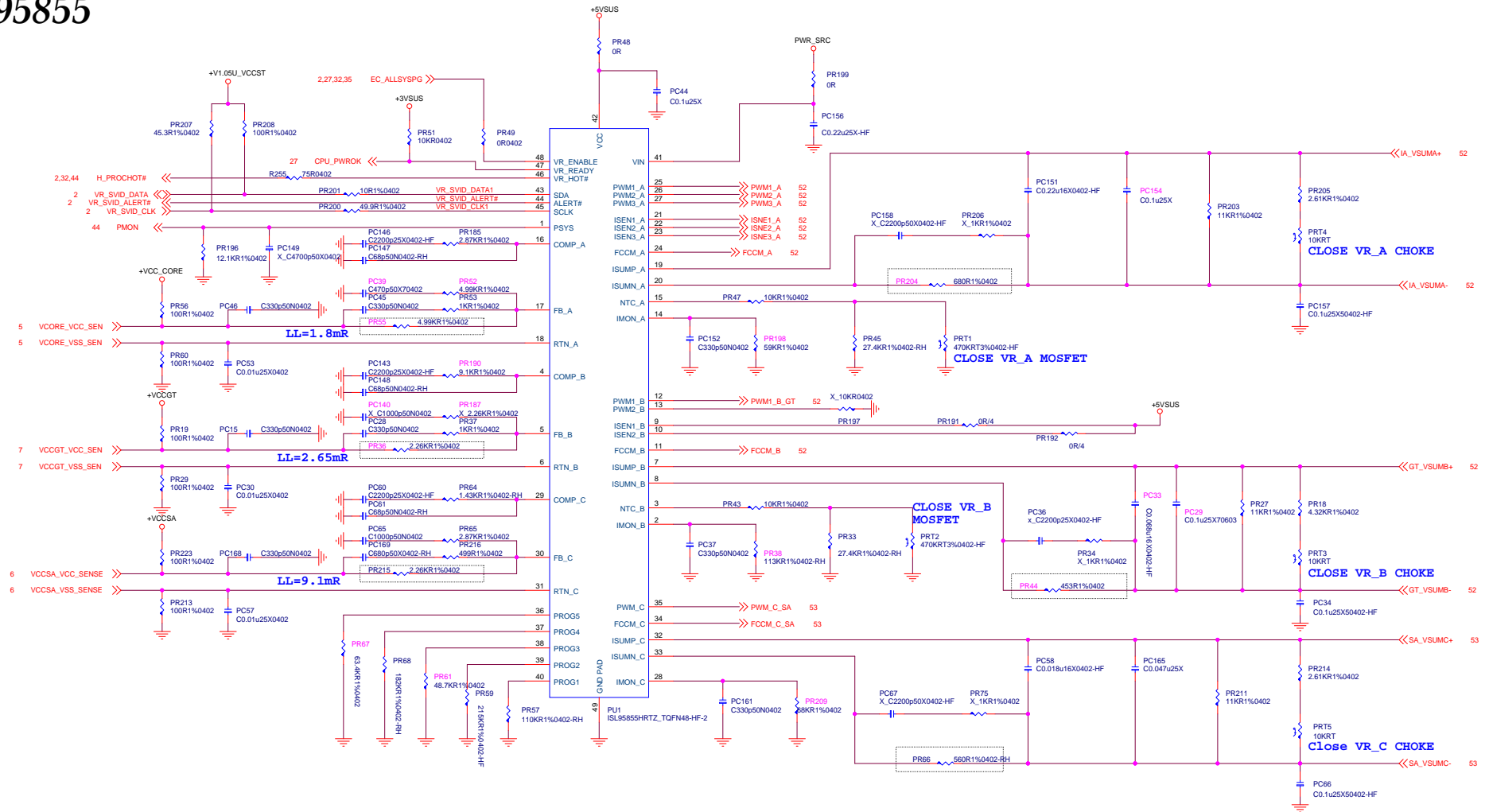


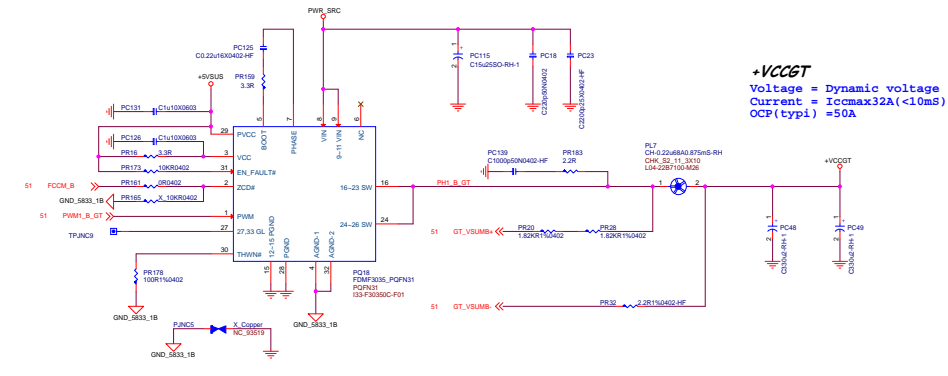
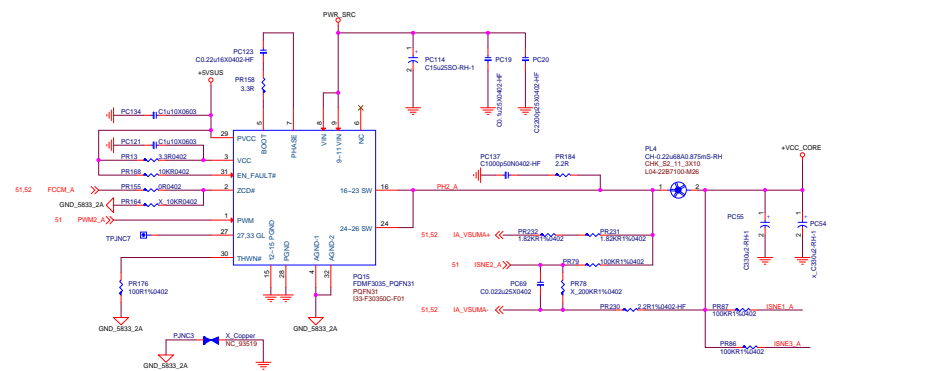
NC

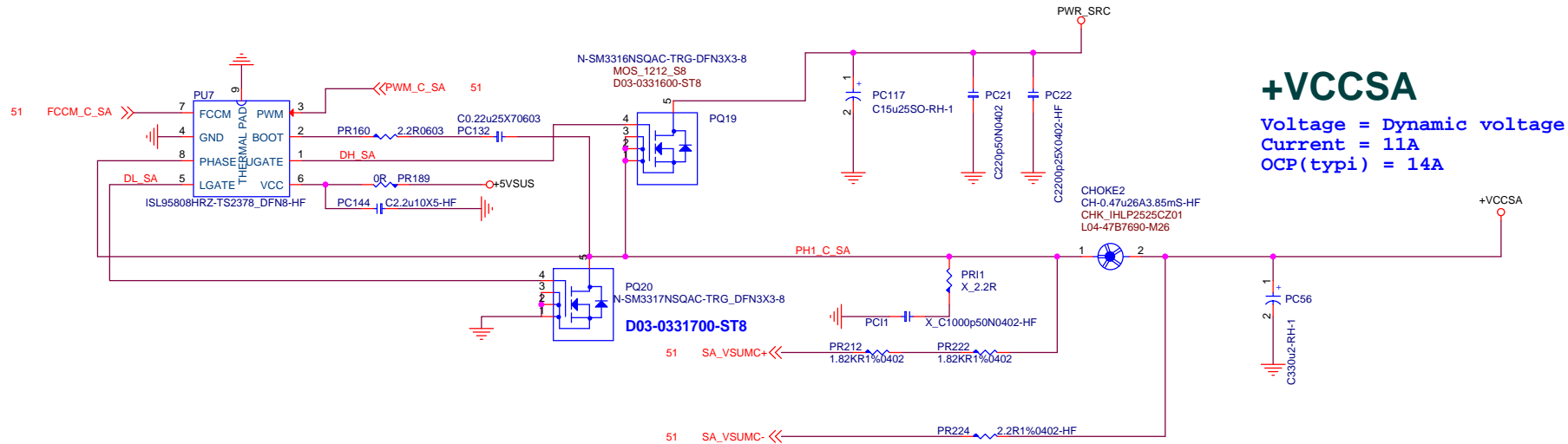
 MICRO-STAR INT'L CO., LTD.	
Title NVDD PHASE 1~4	
Size	Document Number MS-16JF/179F
Date:	Sheet 50 of 61 Rev 0A

Skylake H-line 42 45W

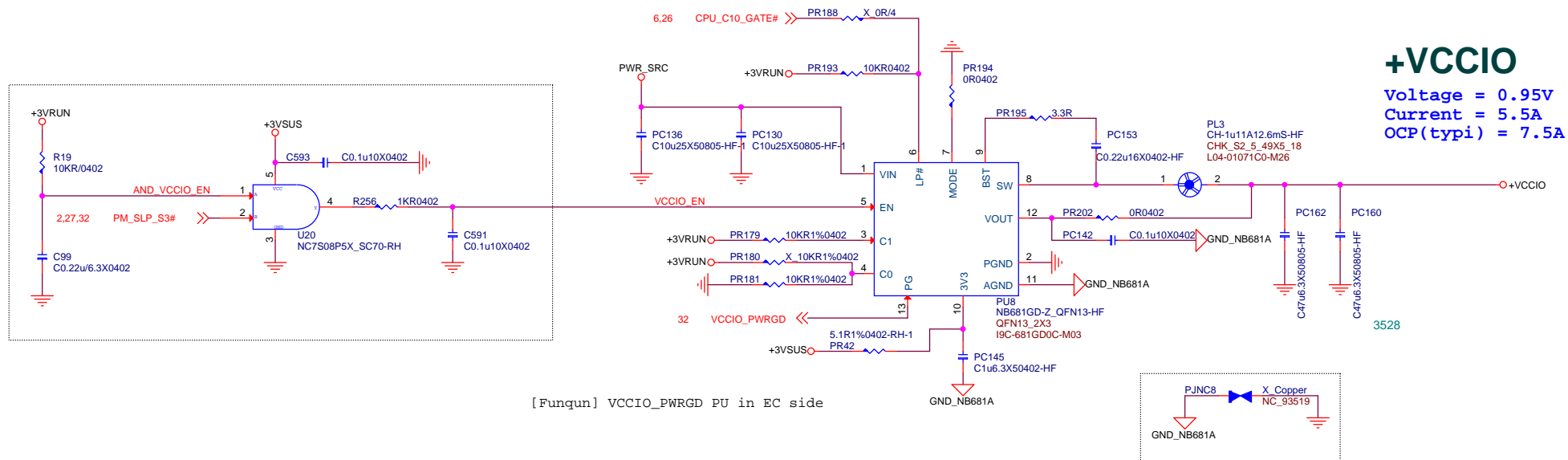
ISL95855



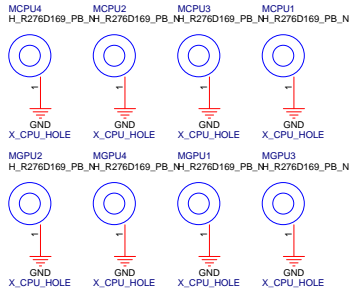




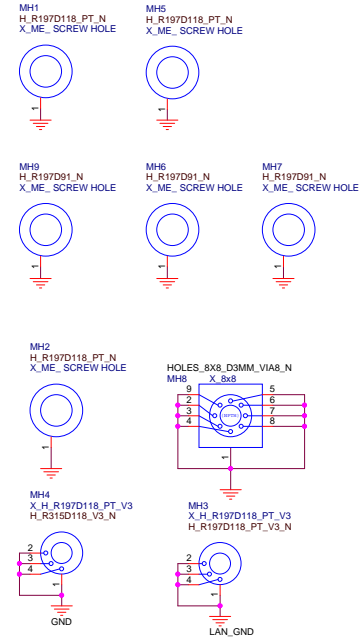
Power Sequence spec tCPU27 :
 CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 240 us



CPU/GPU Holes



OD 2.3



Top Spring

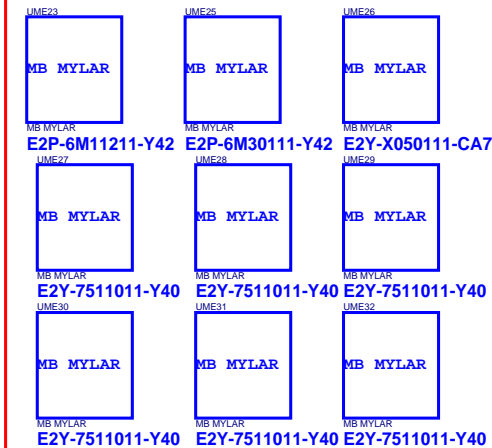
E23-1011040-CA7

E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7

BOT Spring

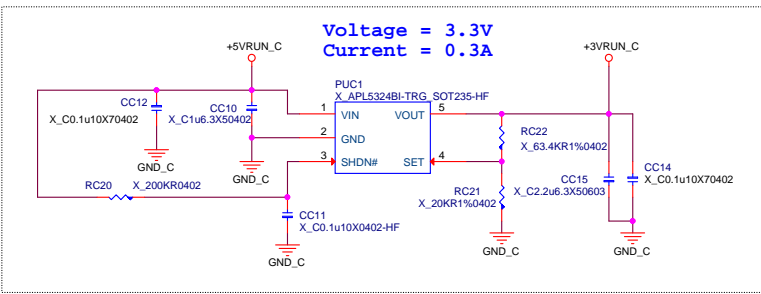
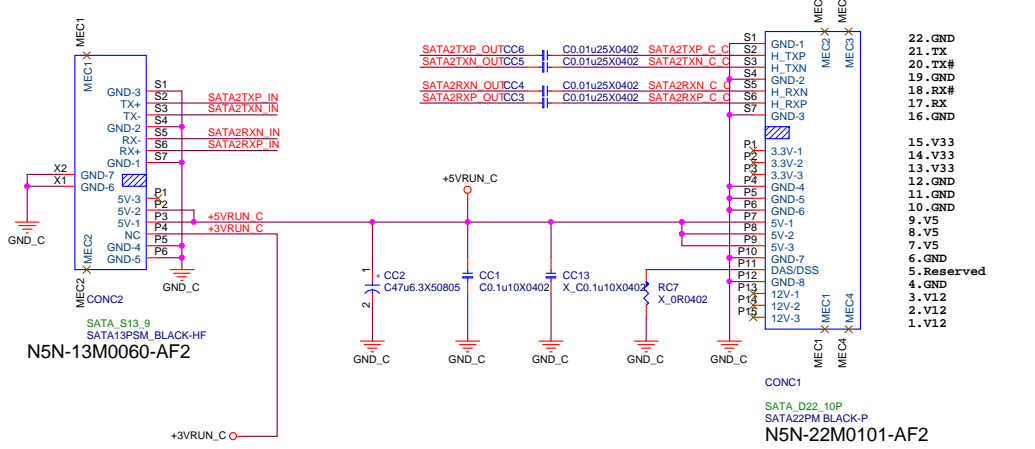
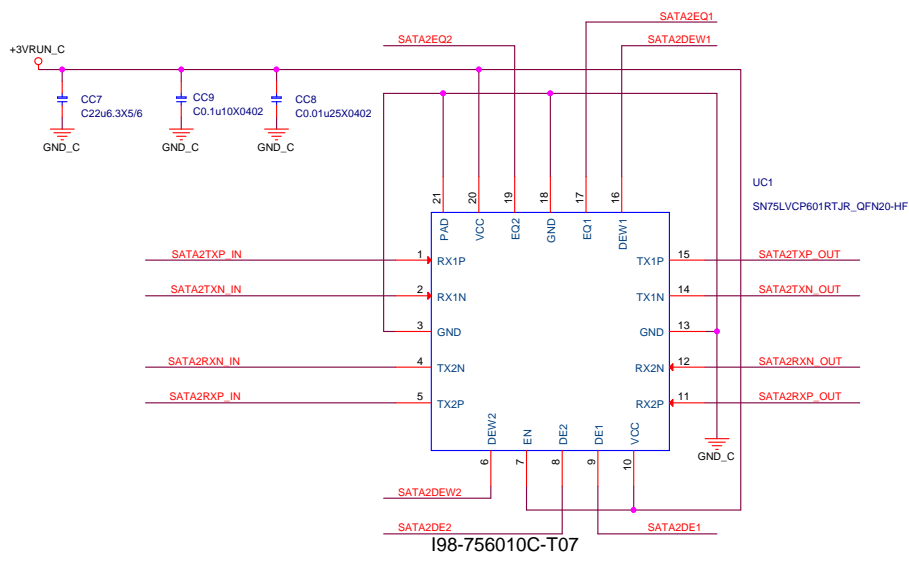
E23-1011040-CA7 E23-1011040-CA7

Only 16M3



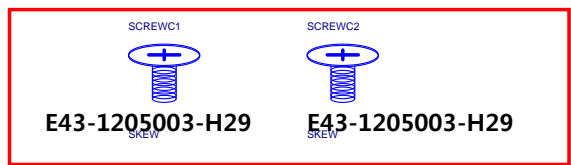
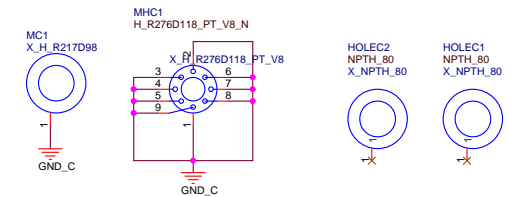
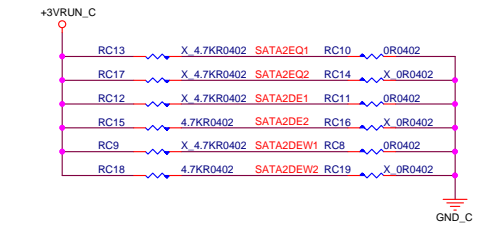
PDO-16JF10A-H73

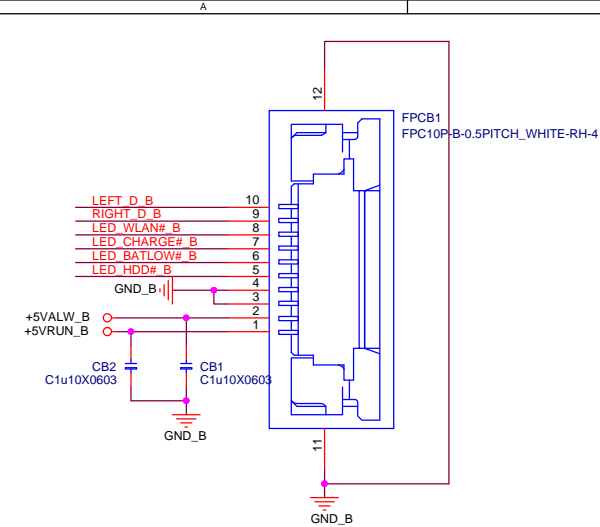
ODD SATA HDD



TX and RX EQ and DE Pulse-Duration Settings

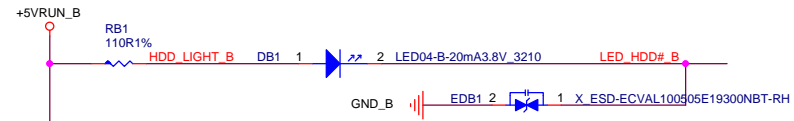
DE1 OR DE2	CH1 OR CH2 DE-EMPHASIS dB (at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization dB (at 6 Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14
DEW1 OR DEW2	DEVICE FUNCTION → DE WIDTH FOR CH1/CH2		
0	De-emphasis pulse duration, short		
1 (default)	De-emphasis pulse duration, long		



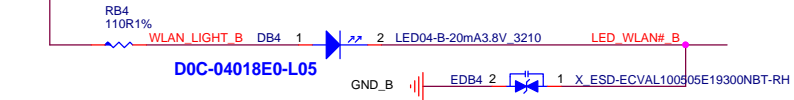


LED for 179F

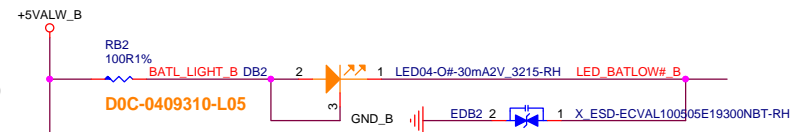
Blue
(HDD)



Blue
(WLAN)



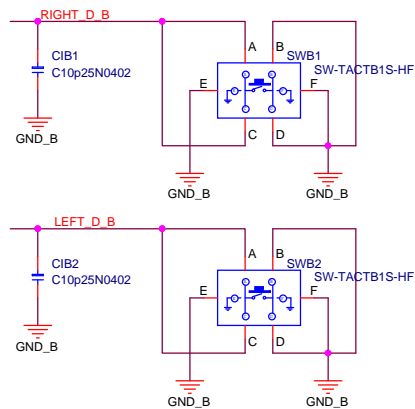
ORANGE
(BATLOW)



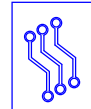
Blue
(CHARGE)



T/P for 179F

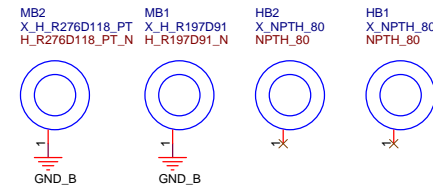


PCBB1



PD0-16JFB0A-H73

PD0-16JFB0A-H73



UMEB1



LEAKAGE_MYLAR

E2P-7910811-G40

UMEB2



MYLAR

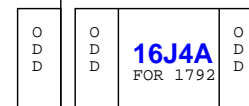
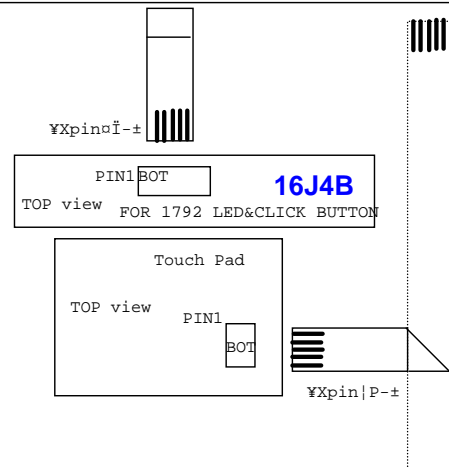
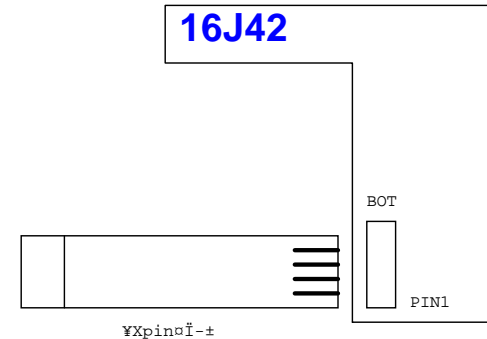
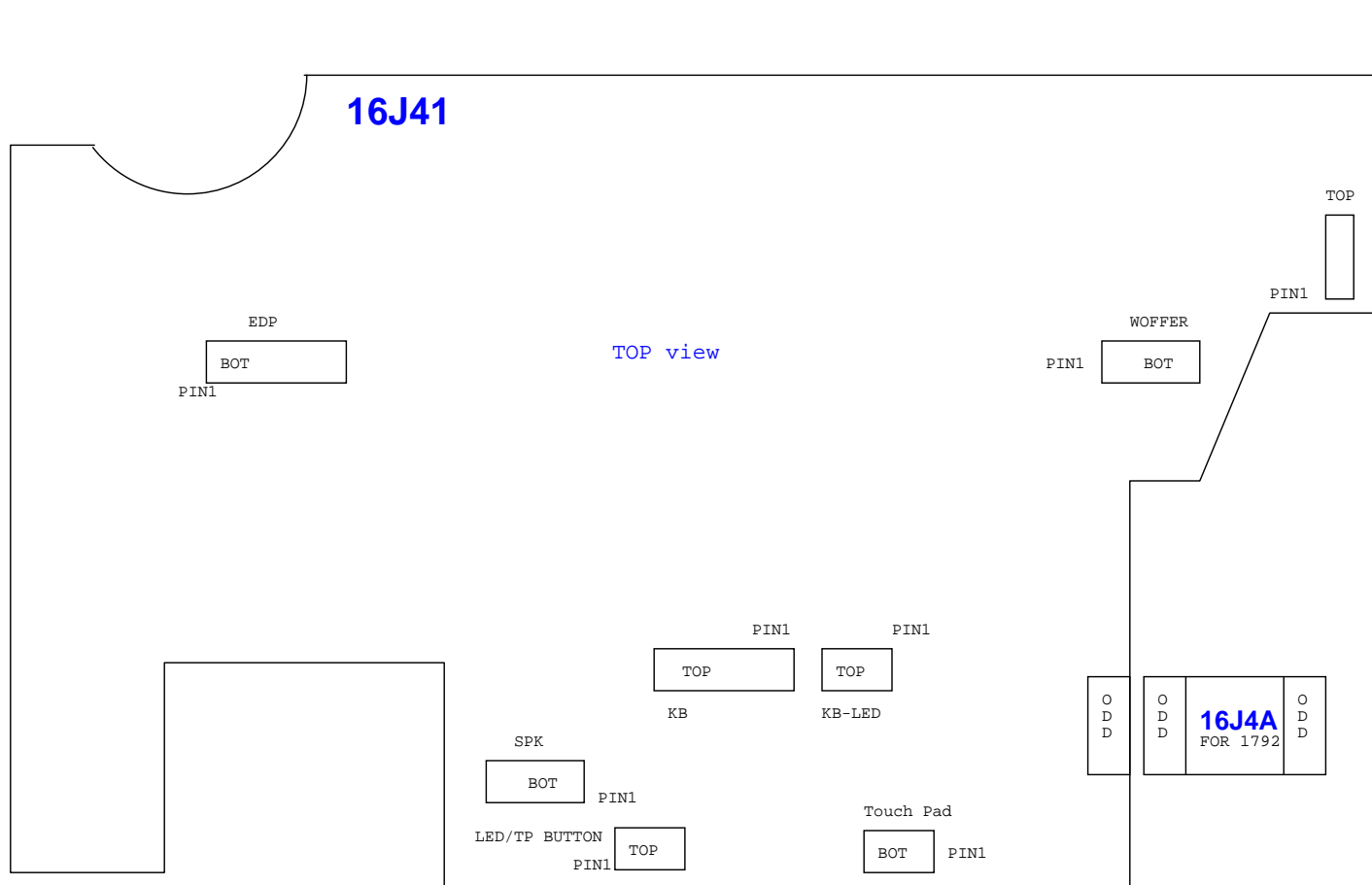
E2P-0113511-G40


16M3 Revome

msi

MICRO-STAR INT'L CO.,LTD.

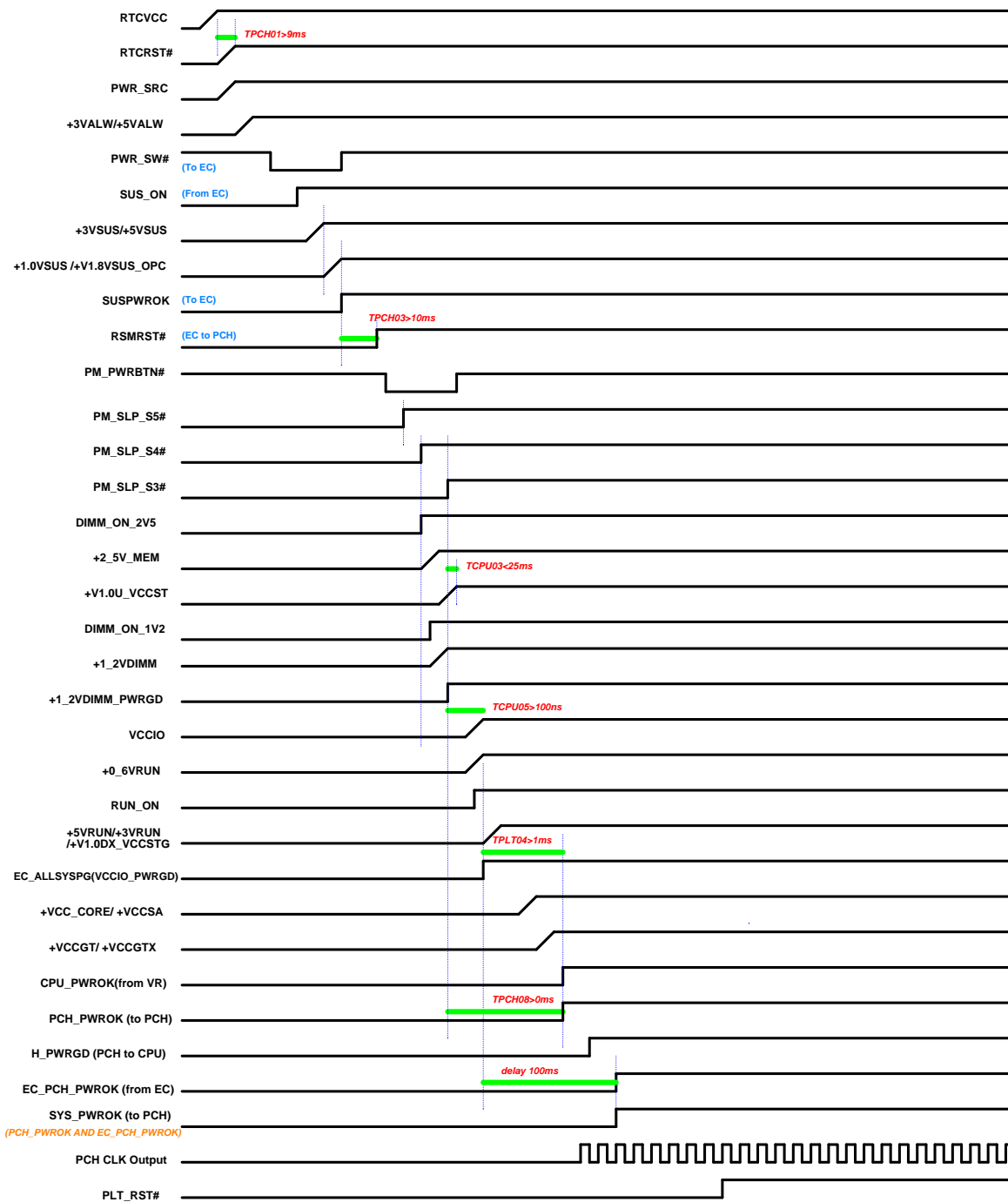
Title		
[B] 1799 LED/ TP		
Size	Document Number	Rev
B	MS-16JF/179F	0A
Date:	Thursday, November 09, 2017	Sheet 57 of 61



		MICRO-STAR INT'L CO.,LTD.	
Title			
VIEW			
Size	Document Number		Rev
Custom	MS-16JF/179F		0A
Date:	Thursday, November 09, 2017	Sheet	58 of 61

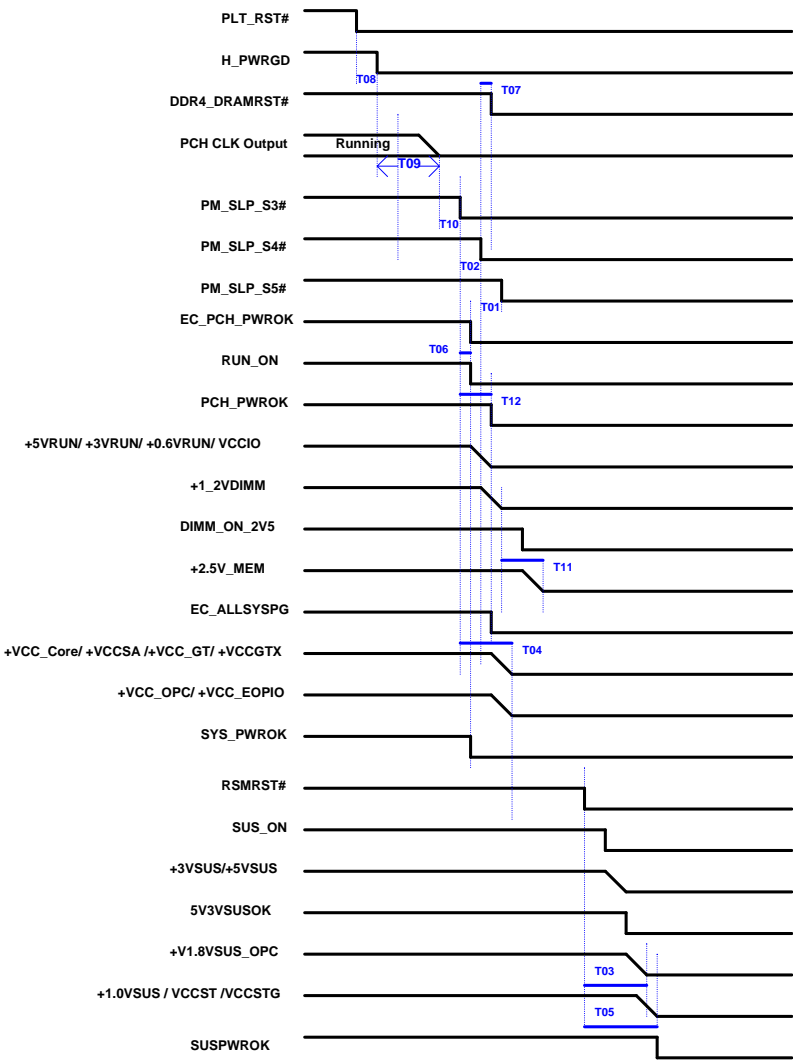
Power on Sequence

G3 -> S0



Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

History

0A		0A		10			
Page	Description	Page	Description	Page	Description	Page	Description
28	REMOVE PU R164,R172,R151,R149	12~17	memory change	R247 ,R441,D8stuff		43	Change R421 from 33R to 22R
		19~21	RC08E,1108E	R147,R464,R4480WY6	6/12		7/7
33	JNC13 CHANGE FOOTPRINT		5/12	U39 change to B07-P021J44-EB3		43	Change C413 & C414 from 20p to 33p
	R176,R412 CHANGE TO JNC29,JNC30	27	Change R111 reference 4.99K to 20K	U43 change to M31-25B6412-GA0		51	Change R135 from 0R to 4.7KR
30	ED10,ED11 PIN4,5 CHANGE NET	30	D3 +3VRUN change to 3V_NV	U13 change to B02-011422C-AD0			Add D13 circuit for power sequence
42	REMOVE G2	49	PR61 :1ohm 0402 >0603 (R11-0010023-W08)	VCCORE:		57	Add D14 circuit for power sequence
			PC64 :1u 0402>0603 (C11-1057613-W08)	PR174 : 470R'453R(R11-4530T22-W08)	6/16	59	Stuff UME2
38	ADD ESD2		PR74 :205Kohm>187Kohm(R11-1873T12-W08)	PR34 : 2.15K'2.43K(R11-2431T12-W08)			Remove all gate
		52	+1VSUS VCC0A8E	PC163 : 0.1u7NC		59	7/13
30	ADD TPS25810 U34			PC48 : 0.1u'0.22u(C11-2242512-M09)			Add UME16 for 16J4 TP Mylar
	ED11 P/N SWAP	33	U17 CPU_POWOK add C to ground	PR164 : 82K'95.3K(R11-9532T12-W08)		54	7/16
28	R144 PU TO 3VSUS	49	PR33'<08E	FBVDDQ		56	Modify PR79 & PR194 from 2.2R to 2.7R
				PR11 : 33.2K'27K(R11-2702T12-W08)		57	Modify PR114 & PR116 & PR113 & PR117 from 0R to 3.3R
5	REMOVE R67	44	CON10 Change to N54-06F1371-SL0	VGT:		60	Modify PR119 from 0R to 2.2R
			CN13 Change to N58-08F0191-SL0	PR144 : 340R'374R(R11-3740T12-W08)		61	Unstuff A board component for 16J4
6	ADD C597	39	Y4 change to D04-0901000-SC6	VCCSA:		36	Unstuff B board component for 16J4
3	REMOVE R74,R72 ,C262			PCS1 : 6800P'0.018u (C11-1832512-M09)		40	7/24
8	REMOVE C597	37	LED--yy'q'9gi-E	PR176 : 91K'93.1K(R11-9312T12-W08)			Stuff UB1 & unstuff UB2 for 1794
						34	20150724 Modify F1 location
25	C646 CHANGE FOOTPRINT	54	PC62 change to C11-4722812-M09	PR147,PR150,PR151,PR152	6/17	38	20150727 Remove BIOS ROM socket
	REMOVE R380 ,R376			PC135,PC136,PC137,PC138			20150727 Remove SW3 & C207
31	DP REMOVE U8 ,ADD Q22,Q23,Q24			0WY6			Modify to 1.0 BOM
				R72 change to L02-1008023-T19			8/6
21	ADD R448 ,R380			U29 change to N-90-GSMS1-RH	6/22	38	Change CPU PN to A0D-6700H15-I06
							PCH PN to B01-HM17005-I06
30	ADD C725,C726						Change R348 from 20KR to 4.7KR
39	PR54,PC57 CHANGE FOOTPRINT						8/17
							Unstuff CON6
41	PC197 0805 CHANGE 0402 FOOTPRINT			ED10, ED11 stuff	6/23		Change BIOS label to G51-N1C0041-A09 for AMI
42	PC91 0805 CHANGE 0402 FOOTPRINT						Change 2N7002 dual PN to D03-65D8L09-D07 for Safety
05	REMOVE R31			E207me0W			8/24
				R2190WY6			Modify DGPU VRAM size from 3G to 6G and strap value
30	U34 CHANGE FOOTPRINT						Change UME16 to un-stuff for ME request
							9/08
29	REMOVE R139,R163			CPU		6/24	Modify GPU HW strap value to correct
33	REMOVE C665 ADD JNC31			PC105,PC106,PC107,PC108,PC109,PC110,PC112,PC113,			11/30
48	REMOVE J24 ,J17,J12,J18			DGPU :			
				PC167,PC169,PC170,PC178,PC183,PC184,PC185,PC187			
49	REMOVE PAD1,PAD5,PAD9,PAD10			Change to C11-1067610-M09			
43	REMOVE G3,G4						
				E2P-6J11211-Y42'K'E	6/25		
48	ADD +1_2VDIMM EMI CAP						
	REMOVE J19,J22			Add E2Y-Z001711-G40*2			
42	ADD PC666			Add BIOS Socket			
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